Simulation Investigations on Fluid/Structure Interaction in the Reflow Soldering Process of Board-Level BGA Packaging

Chun-Sean Lau and Mohd Zulkifly Abdullah

***Abstract*—The objective of the present study is to develop a Fluid/Structure Interaction model of a board-level Ball Grid Array (BGA) assembly for an infrared-convection reflow oven. The infrared-convection reflow oven is modeled in Computational Fluid Dynamic (CFD) software while the structural heating BGA package simulation is done using Finite Element Method (FEM) software. Both software applications are coupled bidirectional using the Multi-physics Code Coupling Interface (MpCCI). The simulation thermal profile is compared with the experiment thermal profile, and they were found to be in good conformity. The simulated flow fields show that the convection mode in an infrared-convection reflow oven played minor effect on heat transfer to the printed circuit board (PCB). The dominant heat transfer mode in an infrared-convection reflow oven is the radiation mode from a quartz heating tube. From the simulation results, the PCB near the edges or corners tended to heat up first at preheating, soaking and reflow stages. The PCB and component experience larges temperature difference in preheating stage. This situation runs the risk of an excessive board warpage. In addition, the maximum von-Mises stress is trapped in the interfaces between solder joint and die, which intend to form the nucleation of initial solder joint crack. This guideline is very useful for the accurate control of temperature and thermal stress distributions within components and PCB, which is one of major requirements to achieve high reliability of electronic assemblies.**

***Index Terms*—Ball grid array assembly, infrared-convection reflow oven, computational fluid dynamic, finite element method.**

I. Introduction

Reflow soldering process has been affected by miniaturization of electronic packages and complicated thermal-mechanical design of a printed circuit board (PCB) assembly. Additional challenge is presented with environmental concerns propelling a rising trend toward lead-free soldering. A lead-free solder requires a narrower range of flow temperatures and workable melt compared with a lead-based solder. Using an inadequate reflow profile may not only result in a high level of thermal stress in the package, but may also result in excessive PCB warpage [1]. Those defects can then result in significant reliability issues in the electronic industry.

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In recent years, a simulation tool for the reflow soldering process greatly helps the electronic manufacturing industry [1]. Therefore, a prediction of the thermal response of the soldering process is crucial for initial parameter design. The popular thermal response analysis at the package level is based on the finite-element method (FEM). Shen *et al.* [2] and Inoue and Koyanagawa [3] built the FEM model to obtain the temperature distribution of a ball grid array (BGA) package for the reflow process. The average heat-transfer coefficient (h_{avg}) was calculated using experimental equations for multiple impinging jets. However, the experimental results obtained by Illés [4], [5] showed that the heat transfer coefficient (h) was inconsistent within the reflow oven.

Thus, to investigate the thermal response and thermal stress within the BGA assembly, undertaking a thermal investigation at the board-level BGA assembly is necessary. This investigation can be accomplished by considering the conditions in the reflow oven and the board configuration. Three mode of heat transfer, such as radiation, convection and conduction occurs during reflow process. Radiative heat transfer occurs from quartz heating tube over the BGA assembly [6]. Hot air circulated by fan inside the oven contact with BGA assembly and heat transfer thought convection mode. Lastly, the heat transfer by conduction within the multi-material BGA assembly. Modeling of radiative heat transfer using Computational Fluid Dynamic (CFD) software has been reported by few authors [7], [8]. Chhanwal *et al.* [7] and Wang *et al.* [8] built CFD model of heating oven for bread-baking process. They found that discrete ordinates (DO) radiation model that takes into account media participation was best suited for problems with localized heat source.

However, not many authors reported multi-physics activities simulation in reflow process, such as the influences of the flow field of a reflow oven to structure model. Lau *et al.* [1] developed thermal coupling method to obtain temperature and thermal stress distribution within solder joints for forced convection reflow oven. The commercial software of CFD and FEM were allowed to be coupled in Multi-physics Code Coupling Interface (MpCCI), which will facilitate high simulation quality. Furthermore, the MpCCI software was utilized in biomedical, nuclear, and aerospace engineering application [9]–[11].

In the present study, a fluid/structure thermal interaction model using MpCCI was developed. This method used to investigate the thermal response and warpage at the board-level BGA assembly in infrared-convection reflow oven. The internal flow of an infrared-convection reflow oven was modelled in CFD software (FLUENT 6.3.26) and a structural heating board level created using FEM software (ABAQUS 6.9). The flow field of the infrared-convection reflow oven was simulated and discussed during the reflow process. The model was validated using experimental measurement data within the acceptable error. Temperature distribution within board-level BGA assembly was analyzed. Finally, the effects of warpage and thermal stress on PCB were discussed.

II. TEMPERATURE AND THERMAL STRESS ANALYSIS

In this section, numerical techniques, such as the fluid/structure thermal coupling method was applied to model the flow field, temperature and thermal stress response at the board-level BGA assembly on the infrared-convection reflow oven. Three important steps are described, namely, the CFD infrared-convection model, board-level structural model and coupling of both models.

A. CFD Infrared-Convection Model

During reflow soldering process, heat transfer takes place by radiation, convection and conduction. The heat-transfer energy (q) from the quartz heating tube to the PCB and the package can be expressed using Eq. (1). The q was calculated using the FLUENT 6.3.26 solver based on the boundary conditions applied at that model. In general, the convection heat-transfer coefficient (h) depends on flow properties, such as velocity, viscosity, and Reynold number of air.

$$q = hA_{heat}(T_g - T_s) + q_{rad} \quad (1)$$

where A_{heat} is the heated area of the PCB or BGA package, T_g is the local fluid temperature, T_s is the wall surface temperature, and q_{rad} is radiative heat energy.

For the symmetrical problem, a three-dimensional (3D) half geometry of the desktop lead-free reflow oven was created, without the board-level BGA assembly, as shown in Fig. 1. The surface and volume meshes were generated using GAMBIT 2.3.16 and exported to FLUENT 6.3.26 for analysis. The mesh size was dense near the board-level BGA assembly, and a tetrahedral grid was used to create the volume mesh. The total number of faces was 533,945 with 256,933 cells. The mesh and time-step sizes used in the current study were optimized and finalized for better accuracy and computational time.

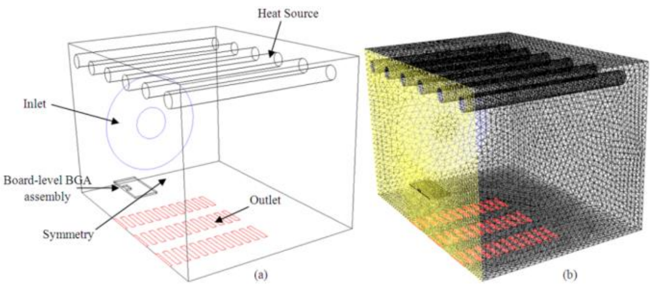

Fig. 1. (a) Three-dimensional half geometry of the reflow oven without the board-level BGA assembly. (b) Meshed with hexahedral grid

FLUENT 6.3.26 provides five radiation models, P-1, Rosseland, Surface-to-Surface (S2S), DO and Discrete Transfer Radiation Model (DTRM) which allows heat transfer simulations. From a previous study, DO model is best suited to model the behavior of the heating source of a quartz heating tube over the surface [7], [8]. The DO model can be expressed by Eq. (2) [7], [12]. Absorption (a) and scattering coefficient (σ_s) are important factor in heat transfer calculation for DO model. Scattering Coefficient of air was assumed zero, and absorption coefficient of air was set as 5 based on infrared transmittance (95%).

$$\nabla.[I(\vec{r},\vec{s})\vec{s}] + (a+\sigma_s)I(\vec{r},\vec{s}) = a\eta^2\frac{\sigma T^4}{\pi} + \frac{\sigma_s}{4\pi}\int_0^{4\pi} I(\vec{r},\vec{s}\,')\phi(\vec{s},\vec{s}\,')d\Omega' \quad (2)$$

The user-defined function profile was developed using the C program based on the actual setting temperature of desktop lead-free reflow oven. The 1.5 m/s was set at a fan inlet, which was measured by using the airflow meter. A symmetrical boundary condition was also defined to reduce the computational time, as shown in Fig. 1. The diffuse faction of a highly polished side wall was set as zero to allow specular reflection from those surfaces. The SIMPLE algorithm was used for pressure–velocity coupling and for the second-order upwind scheme to discretize each control volume for better accuracy.

B. Board-Level Structural Model

In the present study, the sample thermal profile board is constituted by package type BGA (11.0×11.0) mm on a (48.0 ×53.0) mm PCB. As the actual board-level BGA assembly is very complex and could not be modeled in detail, a simplified structural model that considers only the PCB, silicon die, solder layer, and mold was developed [13]. To understand the variation of temperature distribution in the board-level BGA assembly, the thermal diffusion is represented by Eq. (3).

$$\rho C_p \frac{\partial T}{\partial t} = \lambda\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + \dot{q} \quad (3)$$

where λ is the thermal conductivity of the PCB or the package and $\dot{q}$ represents the convectional heat transfer energy per volume into the system. $\dot{q} = q/V$, and q already explained in Section II.A.

In multi-material structures, the temperature distribution within a board-level BGA assembly is simulated using FEM based on the structural solver ABAQUS 6.9. In the current study, the coupled temperature–displacement step was used for temperature and thermal stress analysis. The induced moisture content in the previous process was initially disregarded [14], [15]. Thus, stress-free temperature was assumed at initial room temperature. The silicon die and mold were modeled as linear isotropic materials. The FR-4 PCB was modeled as linear orthotropic material, and the solder joint was modeled as a temperature-dependent material. The summarized thermal and material properties used in the model are reported by Lau *et al.* [16].

For symmetry problem, the board-level BGA assembly comprised a half of the entire PCB, as shown in Fig. 2. Meshing was performed using C3D8T hexahedral element with 2,910 nodes and 1,818 elements. The node in the center of the PCB was constrained to the boundary conditions

U_x=U_y=U_z=0 to prevent free-body translation. A uniform temperature of 300K (room temperature) was set as the initial temperature in ABAQUS. After the initial step, the applied surface heat transfer coefficient and film temperature were provided using a CFD code, which already explained in Section II.A.

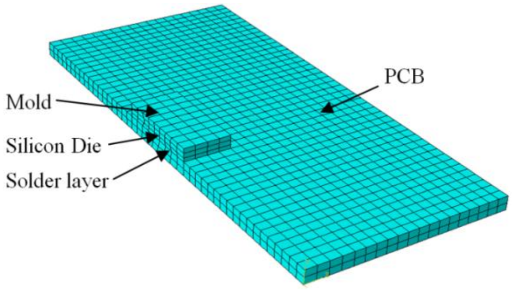

Fig. 2. Computational meshes in the board-level structural model

C. Coupling of CFD and Structural Models

MpCCI 3.1 was applied for bidirectional coupling of the CFD and the structural solvers. In this approach, the fluid solver (FLUENT 6.3.26) and the structural analysis codes (ABAQUS 6.9) were simultaneously ran. Coupling information was exchanged during the simulation. Interpolation was used to transfer quantities between the fluid and structural meshes [10]. The coupling surface comprised the entire surface of the structure. The coupling quantity data were time-step size, film temperature, wall heat-transfer coefficient, and wall temperature of the structure [1]. The time step of 0.1 s was proven to be optimum according to the courant number within the domain that did not exceed a value of 40 in the most sensitive regions [12]. Data exchange also occurred every 0.1s, with FLUENT sending the film temperature and surface heat-transfer coefficient to ABAQUS and ABAQUS sending the current wall temperature to FLUENT. The simulation for the time period from *t*=0s to *t*=261s consumed approximately 24 h of wall clock time. More information is available in the MpCCI 3.1 documentation [17].

III. Experimental Procedure

This section describes the experiment conducted to validate the thermal-coupling numerical model. The desktop lead-free reflow oven was used in the experiment. The reflow oven was appropriately programmed into the following temperature sections: preheating, soaking, reflow, peak, and cooling, to obtain a profile for lead-free soldering process. The board-level BGA assembly was subjected to controlled heat, which melted the solder balls, and then subjected to controlled cooling to permanently form the joint in the infrared-convection reflow oven.

The experiment setup as shown in Fig. 3 was performed for temperature measurements of PCB substrates during the reflow process. A K-Type Thermocouples (TCs) were connected at desired location, as shown in Fig. 4. The TCs were attached with aluminium tape. It is imperative that the tape be pressed so firmly over the TCs bulb that a perfect image transfer of the tip can be identified. Next, a piece of Kapton tape over the lower part of the aluminium tape is used to further prevent lift off. Room temperature was maintained at 300K throughout the experimental verification using an air conditioner. A data acquisition module was used to connect TCs and directly interfaced with the personal computer, as shown in Fig. 3. These data were used to validate the simulation results, as explained in Section IV.A.

Fig. 3. Experiment setup

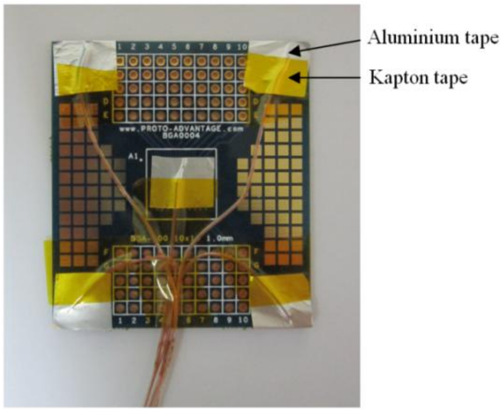

Fig. 4. Location of the thermocouple attachment on the PCB

IV. Result and Discussion

A. Experimental Validation

The objective of this comparison is to validate the thermal response of thermal-coupling numerical model. The temperature setting in the simulation is set according to the reflow oven setting temperature, which controlled by thermostat. Thermostat keeps the heating source of reflow oven according to the set point, as shown in Fig. 5. Besides, Fig. 5 also shows the comparisons of simulation profile against the experimental results with 95% confidence interval.

For experiment, profiles are measured by a K type-thermocouples located at the four corner of the PCB and repeated 5 times; while simulated profiles are taken from a same location. K type-thermocouples connected to data acquisition module and interfaced with personal computer was used to record temperature profile. Both profiles show that the temperatures on PCB are lower than setting temperature. The time delay exists indicate that the measuring points do not instantaneously heat up and reach the setting temperature. Besides, the small percentage error shows that the numerical simulations are in good agreement with the experimental data. Thus, we can conclude that profile simulation is feasible for the infrared-convection reflow oven.

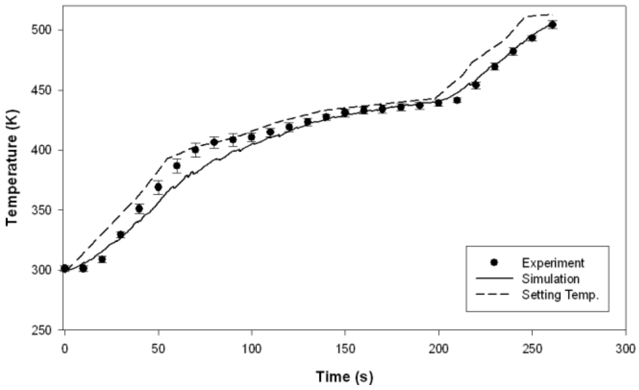

Fig. 5. Simulation and experimental temperature profile

B. Flow Characteristic of an Infrared-Convection Reflow Oven

The air flow in infrared-convection reflow oven is shown in Fig. 6 and exhibits the velocity change, which depend on the position of the reflow oven. The velocity at the exhaust port was higher (4.79 m/s), followed by velocity at inlet fan (1.5 m/s). The velocity at PCB surface is around 0–0.9 m/s, which show hot air circulated by fan inside the oven contact with BGA assembly and heat transfer thought convection. Since convective heat-transfer coefficient depends on flow velocity, convection mode in infrared-convection reflow oven play minor effect on heat transfer to PCB. Radiative heat transfer from quartz heating tube (infrared) to the PCB is the dominant heat transfer mode in infrared-convection reflow oven.

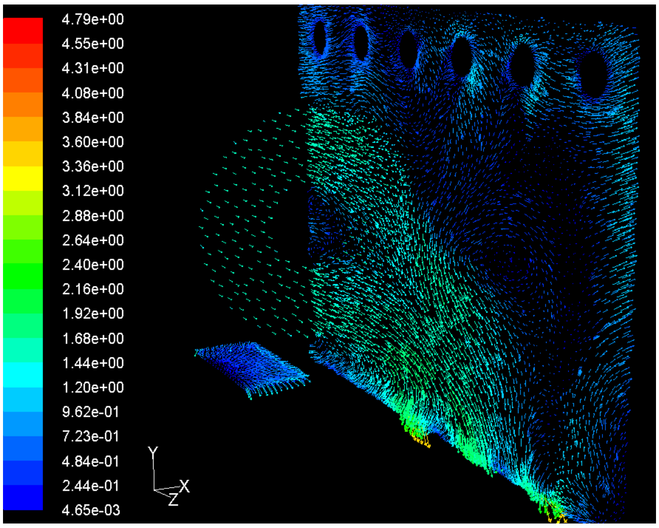

Fig. 6. Velocity vector around the reflow oven at 200s (Unit: m/s)

The surface heat transfer coefficients are different at different location, as presented in Fig. 7. The simulation results show that the PCB consist of surface heat transfer coefficient which around 48 $W/m^2.K$ compares to other locations such as, at the heat sources. These surface heat transfer coefficient results are transfer to structure model to observe the changes of temperature and thermal stress in the board-level BGA assembly.

C. Temperature Distribution within Board-Level BGA Assembly

Fig. 8 shows the temperature distributions in symmetry of board-level BGA assembly of the reflow process. In practice, heating part of reflow thermal profile can be divided into three stages, namely, preheating, soaking, and reflow stages. From the simulation results, the PCB near the edges or corners tended to heat up first at all the stages, consequently temperature differences between the BGA packages and PCB. Cool point occurs at center of BGA packages, whereas hot point occurs at corners of PCB. The maximum temperature difference should not exceed 20 ℃, which reported by Belov *et al.* [18]. Exceeding this limit will result in excessive board warpage. The excessive board warpage cause gaps forming between packages and PCB.

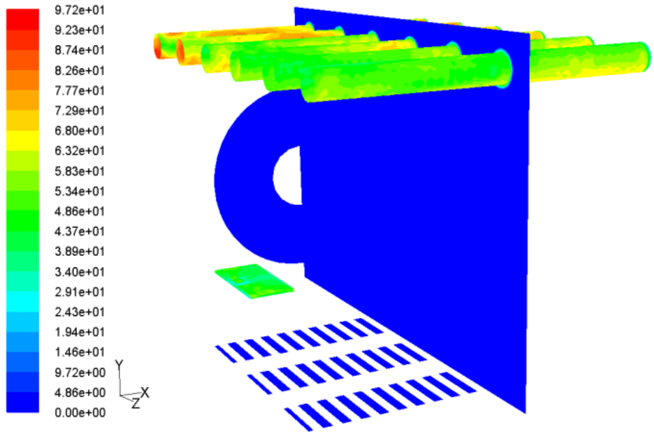

Fig. 7. Surface heat transfer coefficient contour of half of reflow oven. (Unit: $W/m^2.K$)

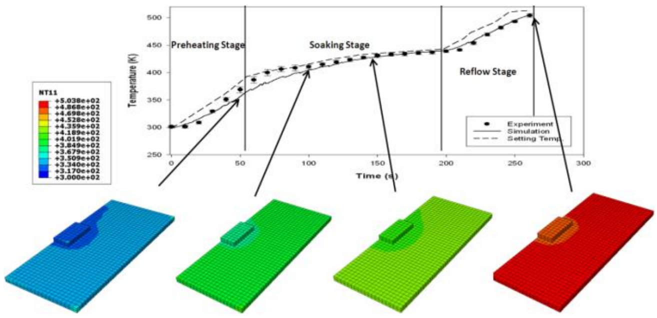

Fig. 8. Temperature distribution contour of the half board-level BGA assembly (Unit: K)

In present study, the worst temperature difference at 29 ℃ was found in preheating stage. The high rates of heat transfer to assembly during preheating stage cause large temperature differences. This results a PCB to warp during preheating stage. Similar results were also observed by Mittal *el al.* [15]. To reduce this defect, slow ramp-up rate is recommended to minimize the temperature gradients across the BGA assembly.

D. Thermal Stress Distribution within BGA Package

The simulation results show that von-Mises stress within BGA package for the non-uniform temperature condition. The von-Mises stress increased with the rising of temperature, as shown in Fig. 9. When the BGA assembly is heating up, it causes a large bending deformation. The thermal stress exists at the interfaces of different materials because of the mismatch of a variant coefficient of thermal expansion (CTE). Fig. 9 also shows the maximum thermal stresses trapped in the interfaces of silicon die and solder layer.

The maximum von-Mises stress occurs at reflow stage, which around 233.7 MPa, as shown in Fig. 9. Besides, the von-Mises stress of solder joint just underneath the die is around 156 MPa. For most experiment results, it was found [19] that the row of joints just outside or just underneath the die edge failed first; this substantiates the present simulation results. For instance, the solder ball root will form the nucleation of initial crack and degrade the thermal cycle life time. However, the stress will be alleviative in the solder joint when the baking is performed after the solder reflow process.

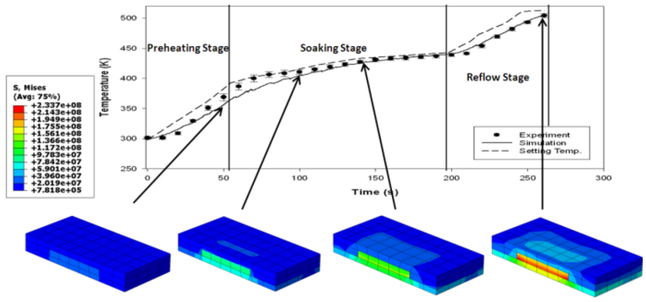

Fig. 9. Von-mises stress contour on BGA assembly (Unit: Pa)

V. Conclusion

This paper outlines a methodology of thermal coupling method for board-level BGA assembly for an infrared-convection oven. In the present study, a thermal coupling method using the code coupling software MpCCI was utilized. The infrared-convection reflow oven was modeled in FLUENT 6.3.26 while the structural heating BGA package simulation was done using ABAQUS 6.9. The simulation results were compared with the experiment results, and they were found to be in good conformity. The flow fields showed that the convection mode in infrared-convection reflow oven played minor effect on heat transfer to PCB. The dominant heat transfer mode in infrared-convection reflow oven was radiation mode. The surface heat transfer coefficients were depending on oven location during the reflow process. The surface heat transfer coefficient of PCB was around 48 W/m^2.K. From the simulation results, the PCB near the edges or corners tended to heat up first at all the stages. The PCB experienced temperature difference at 29 ℃ in preheating stage, give a high risk in excessive board warpage. The maximum von-Mises stress of solder joint just underneath die occurred at reflow stage, which around 156 MPa, tended to cause the solder joint cracking issue. Lastly, study on the package-level BGA assembly will also be interesting in future study.

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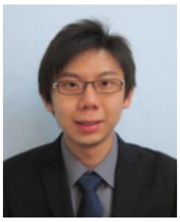

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