An Ultra High Speed Digital 4-2 Compressor in 65-nm CMOS

Peiman Aliparast, Ziaadin D. Koozehkanani, and Farhad Nazari

***Abstract*—The presented work deals an ultra high-speed CMOS 4-2 compressor which is an essential part in fast digital arithmetic integrated circuits. Current-mode techniques have been used to improve the overall performance of the compressor. New fully differential proposed circuit improves delay to less than 37% also reduces occupied area in comparison to other high-speed conventional compressor circuits. To evaluate the performance of the proposed circuit, conventional gate level structure has been chosen and all of the circuits have been simulated in 65-nm IBM CMOS process with 1.2V power supply voltage.**

***Index Terms*—Digital logic, 4-2 compressor, CMOS, high speed, current-mode.**

I. Introduction

With ever-increasing possibilities that VLSI systems provide to realize high-speed digital building blocks, there is a trend toward using digital units to implement processing algorithms even for executing the tasks that were originally analog such as front-end communications. Microprocessors and digital signal processors rely on efficient implementation of fast arithmetic logic units to execute dedicated algorithms such as convolution and filtering [1], [2]. Adders and multipliers are most frequently and widely used arithmetic cells in realizing these processors. In most of these applications, multipliers dictate the overall performance of the system when speed and power consumption are considered as limiting factors. At the circuit design level, there is a great potential for optimization of these building blocks by voltage scaling or application of new CMOS logic styles for the implementation of its embraced combinational circuits [3]. A fast array or tree multiplier is typically composed of three subcircuits:

1) A Booth encoder for the generation of a reduced number of partial products.
2) A carry save structured accumulator for a further reduction of the partial products' matrix to only the addition of two operands.
3) A fast carry propagation adder (CPA) [4] for the computation of the final binary result from its stored carry representation.

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Among these subcircuits, the second stage of partial product accumulation, often referred to as the carry save adder (CSA) tree [5]-[7], contributes most to the overall delay and a high fraction of silicon area. Therefore, increasing the speed of CSA subcircuits is crucial to improve the performance of the multiplier. Early designs of CSA tree used the Dadda's column compression technique [8] with the 3-2 counters, or equivalently the full adders to reduce the partial product matrix. To reduce the delay of the partial product accumulation stage, 4-2 compressors have been widely employed nowadays for high speed multipliers. Because of their regular interconnection, these 4-2 compressors are ideal for the construction of regularly structured Wallace tree with low complexity [7]-[9].

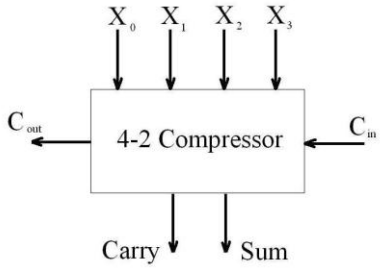

Fig. 1. Block diagram of a 4-2 compressor.

Several 4-2 compressor circuits have been proposed for high-speed applications [3]. In this paper, we begin with a brief introduction of conventional compressors which are composed of two full adders and each full adder optimized in gate level to achieve high speed. After investigating the performances of this 4-2 compressor architecture and their underlying building modules, a new very high speed current mode fully differential 4-2 compressor is proposed. The 4-2 compressors constructed with this current mode technique exhibit superior speed efficiency comparing to other configurations.

II. The Conventional 4-2 Compressor Structure

4-2 compressor has five inputs and three outputs, as shown in Fig. 1. The four inputs X_0, X_1, X_2, and X_3, and the output have the same weight. C_{in} is the output carry of preceding module and C_{out}, the carry output of current stage is fed to the next compressor. The output Carry is weighted one binary bit order higher. The compressor is governed by the following basic equation:

$$X_0 + X_1 + X_2 + X_3 + C_{in} = Sum + 2.(Carry + C_{out}) \quad (1)$$

Besides, to accelerate the carry save summation of the

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partial products, it is imperative that the output C_{out} be independent of the input C_{in}.

The conventional architecture of a 4-2 compressor consists of two serially connected full adders, as shown in Fig. 2(a). Straightforward implementation of this circuit leads to a long critical path delay. Also because of uneven delay profiles of outputs from different inputs, the CSA tree constructed from such cells generates a lot of glitches. So, optimization at gate level is suggested to alleviate these problems [3]. The optimized gate level circuit for each full adder has been illustrated in Fig. 2(b). For NAND gates in this Fig, CMOS static circuits and for realizing XOR gates, transmission gate (TG) circuits have been used. In overall for implementing 4-2 compressor with this method, 72 transistors are required.

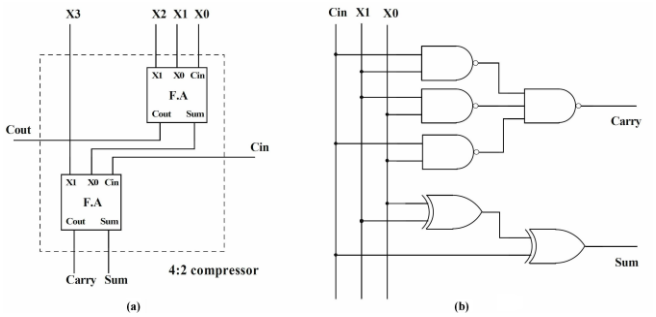

Fig. 2. (a) Convential 4-2compressor scheme, (b) gate level strucure of a full adder.

III. Proposed New 4-2 Compressor Structure

In this section, we describe the new method for implementing 4-2 compressor of Fig. 2(a). This method is based on current mode circuits and adds the currents in analog form.

A. New Full Adder Architecture

If we consider the operation of a full adder, we can replace it with a current mode digital to analog converter (DAC) which produces a current proportional to the inputs of full adder. Table I shows the truth table of the operation and the amount of output current. If we examine DAC current column in Table I and the state of outputs Sum and C_{out} we can change it to a simpler from as shown in Table II. If we pay attention to this truth table, we can easily set the required output bits of full adder. The design procedure is as follow: according to the Table II it is enough that for currents higher than 1.5I with proper margin, we set C_{out} to 1 and if the current is odd we will set Sum to 1. To do this, it is enough to decrease 2I from DAC current when the DAC current is more than 2I. So in this manner, we can compare the output current of the DAC with corresponding currents and set the required bit and when DAC current is less than 2I we compare it with 0.5I. In this case, if it is higher than 0.5I we will set Sum to 1. For comparison of currents we have used two series current source that one of them works as a source and the other one works as a sink. It is clear that if the source current is more than the sink, voltage of the middle node goes to high and vice versa. Fig. 3 illustrates the proposed structure for a full adder.

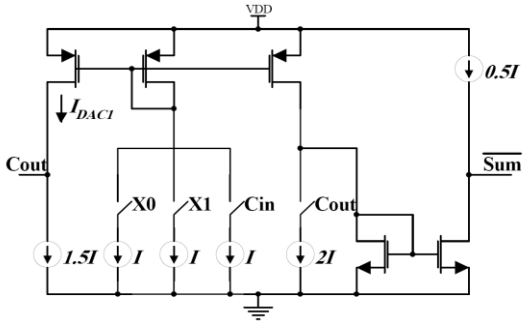

Fig. 3. Proposed new full adder structure.

TABLE I: Truth Table of the Full Adder

C_{in}	X_0	X_1	DAC Current	Sum	C_{out}
0	0	0	0	0	0
0	0	1	I	1	0
0	1	0	I	1	0
0	1	1	2I	0	1
1	0	0	I	1	0
1	0	1	2I	0	1
1	1	0	2I	0	1
1	1	1	3I	1	1

TABLE II: Simplification of Table I

DAC Current	Sum	C_{out}
0	0	0
I	1	0
2I	0	1
3I	1	1

B. New 4-2 Compressor Architecture

Considering the structure of a 4-2 compressor which is constructed using two full adders (Fig. 2(a)). I_{DAC1} and I_{DAC2} are analog currents corresponding to the outputs of each full adder. To realize this compressor the full adder structure proposed in section II. A. has been used (Fig. 3). But note that the Sum output of first full adder is directly connected to second full adder so there is no need to current to voltage conversion. By subtracting $2I$ from I_{DAC1} current corresponding to the Sum output of first full adder could be created and the use of an additional comparator could be avoided. Fig. 4 illustrates the proposed structure for 4-2 compressor.

At first, input bits X_0, X_1, X_2 produce the C_{out} then using C_{out} bit, first full adder DAC current (I_{DAC1}), also C_{in} and X_3 bits, the Carry output is generated. Finally, Carry and second full adder DAC current produce the Sum bit. To understand how this circuit operates, we use one row of truth table as an example which is shown in Table III. For first full adder consider inputs as $X_0 = 1$, $X_1 = 0$, $X_2 = 1$, so in the circuit of Fig. 4, switches X_0, X_2 will be closed and switch X_1 will be open and it results in $I_{DAC1}=2I$. To generate C_{out}, it is enough to compare this current with 1.5I. Because, it is higher than 1.5I then C_{out} will be 1. Now, for the inputs of second full adder considering $C_{in}=1$, $I_{DAC1}=2I$ and $X_3=1$, causes switches

X_3 and C_{in} to be closed. Also, because of C_{out}=1 the switch C_{out} will be closed. The current I_{DAC2} for this node will be:

$$I_{DAC2} = I_{DAC1} + I + I - 2I \Rightarrow I_{DAC2} = I_{DAC1} = 2I \quad (2)$$

Again this current is higher than 1.5I which leads to $\overline{\text{Carry}} = 0$. As a results, ''Carry'' switch will be closed and current 2I will subtracted from I_{DAC2} and compared to 0.5I. Because 0.5I is higher than zero will cause Sum to be 0. For this example, inputs and the results have been summarized in Table III. The same description can be used for other sets of inputs.

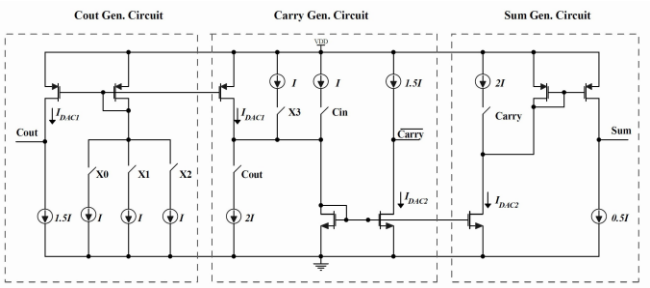

Fig. 4. Proposed new 4-2 compressor architecture.

TABLE III: TRUTH TABLE FOR ONE ROW EXAMPLE OF THE PROPOSED 4-2 COMPRESSOR

C_{in}	X_3	X_2	X_1	X_0	Sum	Carry	C_{out}
1	1	1	0	1	0	1	1

IV. CIRCUIT IMPLEMENTATIONS OF THE PROPOSED 4-2 COMPRESSOR ARCHITECTURE

As shown in Fig. 4, the proposed 4-2 compressor circuits compose of three sections (C_{out} generation circuit, Carry generation circuit and Sum generation circuit). Fig. 5 shows the C_{out} generation circuit. As it is clear from the Fig. 5 each switches of X_0, X_1 and X_2 is replaced with a differential switch. The reason for using differential switch instead of single MOS switch is the advantages of these switches in very high speed operation and producing signal and its complement at same time. On the other hand differential switches can be switch with almost $\sqrt{2}\times\Delta V$ where ΔV is overdrive voltage of MOS transistor, so it can follow very small changes in differential input voltages. For implementation of the current sources in Fig. 4, they have been replaced with current mirror circuits. For a tradeoff between power consumption and speed, we have chosen 2.5μA for the value of I. It is clear that increase of I leads to increase of power and speed of compressor. With same method for C_{out} generation circuit we can implement circuits of Carry generation and Sum generation sections. It is enough that each of switches replaces with differential switches and each current source replace with current mirror transistors. Figs. 6 and 7 show the Carry generation circuit and Sum generation circuit respectively. Fig. 8 shows the output latch scheme that has been used as output load for the proposed 4-2 compressor. Output voltage signal of this circuit can change rail to rail while its input doesn't need a rail to rail voltage signal. Thus it's useful for connected the outputs of the proposed compressor to other static CMOS logic circuits without worry about drawing static current.

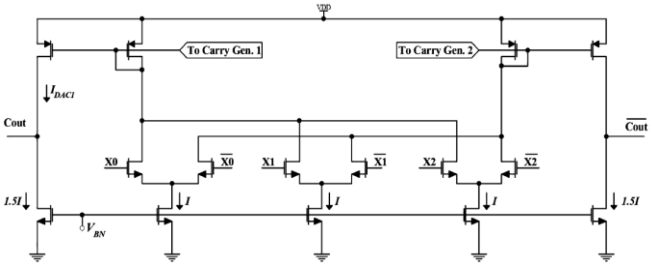

Fig. 5. Cout generation circuit of proposed 4-2 compressor.

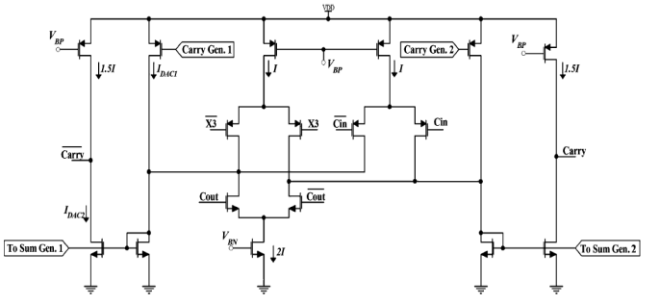

Fig. 6. Carry generation circuit of proposed 4-2 compressor.

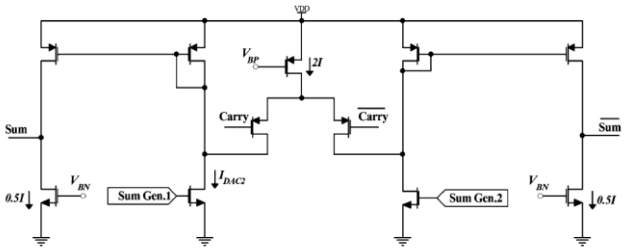

Fig. 7. Sum generation circuit of proposed 4-2 compressor.

V. SIMULATION PERFORMANCE

Fig. 9 shows the simulation environments for the 4-2 compressor. Each input is driven by a minimum size inverter signal. For output load, the proposed 4-2 compressor used latch circuit that is shown in Fig. 8. Conventional compressor structure used a minimum size inverter in output as a load. This consideration provides a realistic simulation environment reflecting the compressor operation in actual applications. The simulation environments of 4-2 compressor (Fig. 9) consist of two cascaded 4-2 compressors. These compressors are running in parallel to simulate an actual compressor stage in the CSA tree. The dashed lines in Fig. 9 indicate the scenario of such potential critical paths with delay time for each of them. For delay numbers, critical path (from input bits to the Sum bit of the neighboring compressor) has been considered. The delay is measured from the earliest input signal converge with its complement to the latest output signal converge with its complement. The worst case delay is largest delay among all input data. For a fair comparison, a conventional structure using two full adders and suggested current steering structure implemented and have been

simulated using a 65-nm IBM CMOS process with 1.2V power supply voltage. Fig. 10 shows simulation results for the proposed compressor in worse case. Random input data with a rate of 1GHz has been fed to the inputs of the compressor. It should be noted that the simulation frequency is not maximum operating frequency of the compressors. In fact the compressors simulated are capable of operating correctly much higher frequency than the simulation frequency.

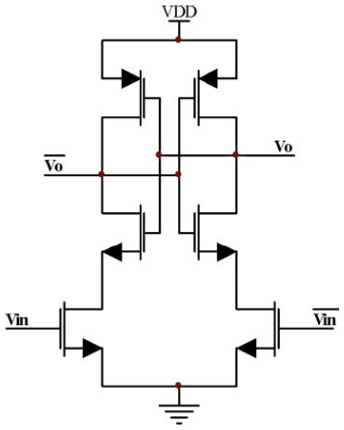

Fig. 8. The output latch circuit scheme.

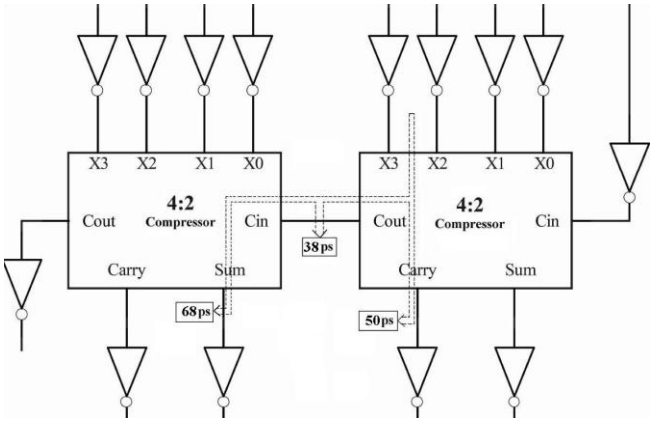

Fig. 9. 4-2 Compressor simulation environment.

Fig. 10(a) shows one of the inputs of the compressor (X0) when it changes state. In worst case condition first valid output after 38ps is Cout which is shown on Fig. 10(b). Then 50ps after input change, Carry will be valid and finally Sum output of the succeeding compressor changes its state after 68ps. Simulation results show a reduced delay less than 68ps which is a considerable improvement compared to conventional architecture. Table IV summarizes the comparison of two simulated structures with explained environment in above.

TABLE IV: COMPARISON OF SIMULATED 4-2 COMPRESSORS

Structure	***Table Column Head***			
	Delay (ps)	***Power (μW)***	***PDP (fJ)***	***Number of Transistors***
Conventional	180	110	19.8	72
Porposed	68	48	3.26	43

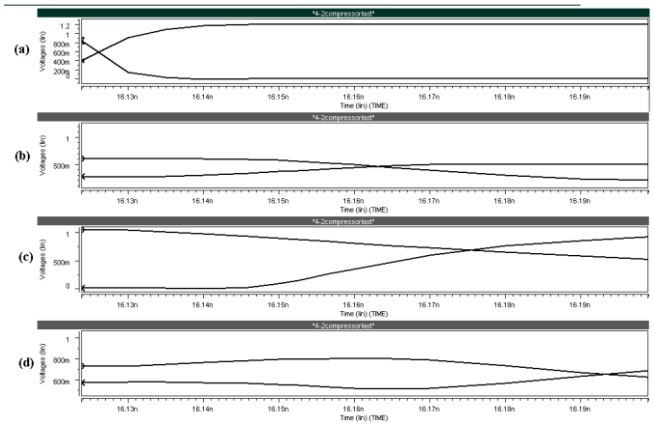

Fig. 10. Simulation results of proposed 4-2 compressor, (a) X_0 and $\overline{X_0}$, (b) C_{out} and $\overline{C_{out}}$, (c) $Carry$ and $\overline{Carry}$, (d) Sum and $\overline{Sum}$.

VI. CONCLUSION

In this work, a new current mode fully differential 4-2 compressor in 65-nm CMOS is presented and compared to a conventional structure compressor. Conventional structure in which the critical path delay reduction is done at gate level has higher power consumption and delay. The proposed compressor shows the highest speed performance, while maintaining lower PDP (power-delay product). Also, the proposed circuit only requires 43 transistors and most of them are minimum size hence this structure occupies smaller area than other high-speed conventional 4-2 compressors. So this is an ideal subcircuit for implementing fast digital arithmetic units.

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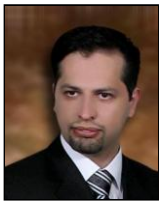

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