# 3D Device Modeling and Assessment of Triple Gate SOI FinFET for LSTP Applications

Kiran Bailey and K. S. Gurumurthy

***Abstract*—The FinFET is a very good candidate for future VLSI due to its simple architecture and better performance when compared to SOI MOSFET. SGOI (Silicon Germanium on Insulator) Recessed Source drain MOSFETs and SOI FinFETs are analyzed by a commercial 3-D device simulator. It is shown that SOI FinFET with Thin Fin widths compared to SGOI MOSFETs Body thicknesses, have better control over short channel effects (SCEs) and reduced power dissipation due to reduced gate leakage currents. By varying the spacer width and the Fin width, device performance is found to improve. The performance of triple gate FinFET has been compared with that of Ultra-Thin Body (UTB) Recessed Source drain SGOI MOSFET in terms of delay, power consumption and noise margin for a CMOS inverter and results indicate the better suitability of SOI FinFET structures for Low standby Power(LSTP) Applications. The SOI FinFET device Sensitivity to process parameters such as Gate Length, Spacer Width, Oxide thickness, Fin Width, Fin Height and Fin doping has been examined and reported.**

***Index Terms*—DIBL, SOI FinFET, SGOI recessed source drain MOSFET, SCEs, subthrehold slope, static power dissipation.**

## I. Introduction

The exponential growth in the semiconductor industry has been achieved through scaling of the MOSFET devices. Several novel nano-scale device structures have been proposed to continue the scaling trends. Such structures include Ultra thin body (UTB) SOI MOSFETs [1], Recessed Source drain SOI MOSFETs [2] and Double and triple gate FinFETs [3]. Previous works that have been reported so far on FinFETs were based on experiments or 2D/3D device simulations [4]-[7] for ideal devices by having abrupt junctions for source and drain regions. Muhammed Nawaz et al [8] has reported the sensitivity of fin width, fin height and fin doping on the drive current and leakage currents of the device. Giuseppe Iannaccone [9] has reported the relevance of CAD tools for understanding the physical mechanisms and performance evaluation and optimization of device structures which includes ballistic strained silicon MOSFETs and silicon nanowire transistors. Mirko Poljak et al [10] have reported the improvement in the dc performance of bulk FinFET in comparison with SOI FinFET by reducing the S/D junction depth. Jerry G. Fossum et al [11] has presented the results of the assessment of SOI and bulk FinFETs suggesting the viability of SOI FinFET. 3D numerical simulations by Burenkov [12] have shown that triple gate FinFETs have better performance compared to double gate structure due to enhanced on current and reduced leakage currents. Kranthi et al [13] has assessed the performance of double and triple gate FinFETs by varying spacer width and lateral doping.

This work focuses on the 3D modeling of Triple gate FinFET architecture using commercially available device Simulation environment and determining the sensitivity of the device to various critical process parameters. The device simulations have been carried out for different Fin body doping, spacer widths, Fin widths and heights, gate lengths and oxide thicknesses. The simulation results are compared with UTB SGOI Recessed source drain MOSFETs and the viability of SOI FinFETs for low power applications is reported.

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## II. Device Structure and Simulation

Ultra-Thin body (UTB) Recessed source drain SGOI device structure [14] and SOI FinFET structures are analyzed and compared using the commercial TCAD Sentaurus device simulator. We have started with a lightly doped P substrate over which a buried oxide (BOX) of 100-150 nm thick was formed.

Device simulations have been performed using hydrodynamic carrier transport model taking into account the band gap narrowing effects, physical effects such as Schokley-Read-Hall (SRH) recombination and Auger recombination effects. The $Si_{0.85}Ge_{0.15}$ material is used for the Fin, Source and Drain regions to enhance the mobility of the carriers. The Off current was defined at $Vgs=0V$ and $Vds=1.1V$ while the On current was defined at $Vgs=Vds=1.1V$.

A 5 nm thin Fin is formed of Silicon Germanium ($Si_{0.85}Ge_{0.15}$) over the Buried oxide. We assumed a Source and drain doping of $10^{20}$ /cm$^3$, with a Gaussian doping profile to a depth of 50 nm. The triple gate FinFET structure has a gate straddling the Fin over a thin 1.2 nm gate oxide as seen in Fig. 1. The Fin Height is set at 50 nm and Fin width 5 nm with the spacer width of 15 nm. The critical process steps for the SOI FinFET device is the formation of 5 nm thin silicon Fin, gate oxide (1.2 nm) growth, polysilicon gate formation(100 nm), Gaussian doping profiles for gradual junctions for source and drain regions with a doping concentration of $10^{20}$/cm$^3$ and spacer formation. The LDD implant and Anti punch-through doping is not necessary as the S/D extensions are formed when the dopants diffuse laterally due to high temperature anneal process after source drain formation. The FinFETs exhibit low gate leakage due to

thicker gate oxides. The SCEs are controlled in these devices in spite of thicker gate oxides since the gate surrounds the channel and the channel is ultra thin.

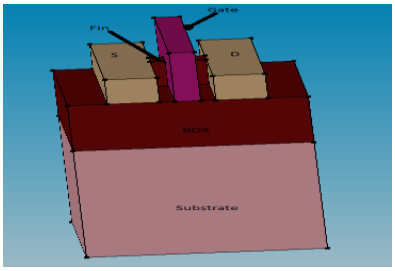



Fig. 1. 3 D device geometry of a 22 nm triple gate SOI FinFET.

## III. Results and Discussion

The transfer characteristic of the 22 nm gate length triple gate FinFET for various spacer widths is shown in Fig. 2. The Fin is undoped (1×1016 cm-3) with a width of 5nm and height of 50nm, Gate oxide thickness of 1.2 nm and nitride spacers of 15 nm. The UTB SGOI Recessed source drain MOSFETs have a novel anti-punch (AP) doping introduced in the source and drain extension regions to control short channel effects. The aim is to control SCEs and thereby control leakage currents thus optimizing for minimum static power dissipation. Table I gives a comparison of the various device electrical characteristics for the 22 nm UTB SGOI Recessed Source Drain MOSFETs and SOI FinFETs.

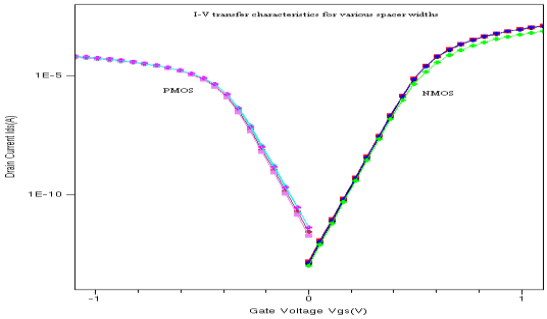



Fig. 2. Tranfer characteristic of a 22 nm triple gate SOI FinFET for various spacer widths.

TABLE I: Electrical Characteristics of the Proposed Triple Gate SOI FinFET and UTB SGOI Recessed Source Drain {NMOS, PMOS} Devices

| Device parameter | AP doped recessed source drain SGOI device[14] | SOI FinFET device |
|---|---|---|
| $L_G$ | 22 nm | 22 nm |
| $T_{OX}$ | 0.9 nm | 1.2 nm |
| Anti punch doping | 1E18 | - |
| Threshold Voltage $V_t$(V) | 0.55,-0.54 | 0.69,-0.455 |
| Ion (uA/um) | 2440, 474 | 1240, 64 |
| Ioff (A/um) | 6.8n, 10n | 0.12p,1.7p |
| $I_{gate}$ (A) | 249.8n, 8.8p | 0.4n, 0.1n |
| DIBL( mV/V) | 122, 110 | 19,60 |
| Subthreshold Slope(mV/dec) | 81.1, 102.9 | 62.84, 64.29 |

### A. Influence of Spacer Width and Fin Doping on Performance of SOI FinFETs:

The influence of spacer width and Fin doping on the device performance was examined to understand the device sensitivity to these process parameters. The spacer width and Fin doping was varied by ±5% and ±10% of the nominal device values. The $I_{on}$ and $I_{off}$ sensitivity is depicted in Fig. 3. The 'on' and 'off' currents show that they are highly sensitive to variation in spacer widths and also Fin doping. Fig. 4 shows the sensitivity of DIBL and subthreshold slope on the Spacer width and Fin doping. It may be observed that DIBL and Subthreshold slope are relatively insensitive to the variation in Fin doping concentration. The doping of the Fin has almost no effect in suppressing SCEs and hence Fin doping is not necessary for these devices. This can be attributed to the better gate control over the channel in FinFET structures. The influence of spacerwidth on DIBL is seen by a 13% decrease in DIBL for a 10% increase in spacerwidth. This is due to the reduced influence of the drain field in the channel due to increased spacer width while the subthreshold slope shows almost no change.

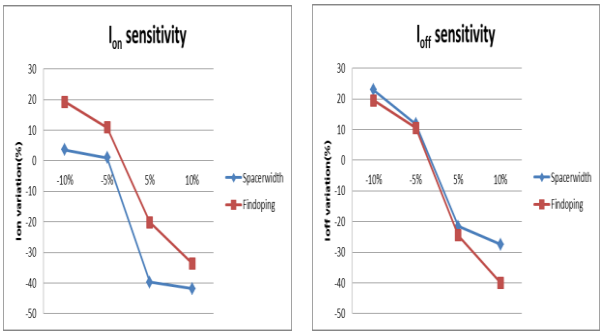



Fig. 3. (a) $I_{on}$ sensitivity (b) $I_{off}$ sensitivity with variation of spacerwidth and fin doping.

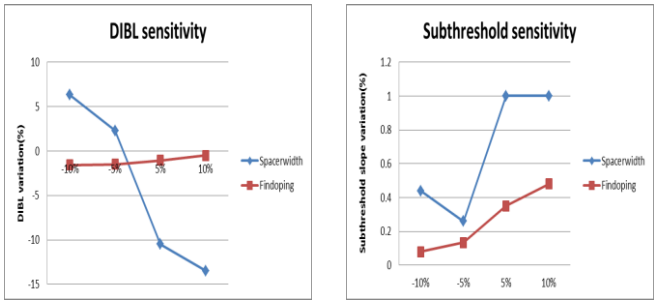
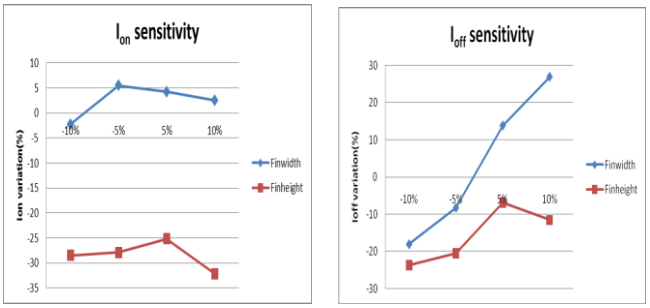



Fig. 4. (a) DIBL sensitivity (b) Subthreshold slope sensitivity with variation of spacerwidth and fin doping.

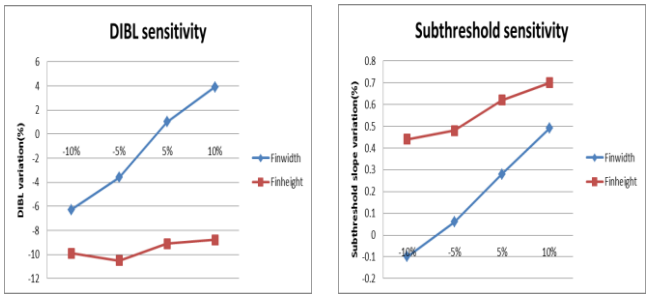
### B. Influence of Fin Width and Fin Height:

Fig. 5 shows the 'on' current and 'off' current sensitivity to variations in the Fin dimensions. The off current is more sensitive to Fin width variation and as can be seen in Fig. 5 (b) leakage current is reduced by almost 20% with reduction in Fin width whereas the on current does not vary by a large factor. As the Fin height is increased, the channel resistance comes down but at the same time the decrease in the drive current may be due to the fact that the source and drain implants cannot penetrate to the buried oxide layer. The DIBL characteristics show an improvement with decrease in Fin width and height whereas the Subthreshold slope remains unaffected by variations in the Fin dimensions as seen in Fig. 6.




(a) (b)

Fig. 5. (a) $I_{on}$ sensitivity (b) $I_{off}$ sensitivity with variation of fin width and fin height.




(a) (b)

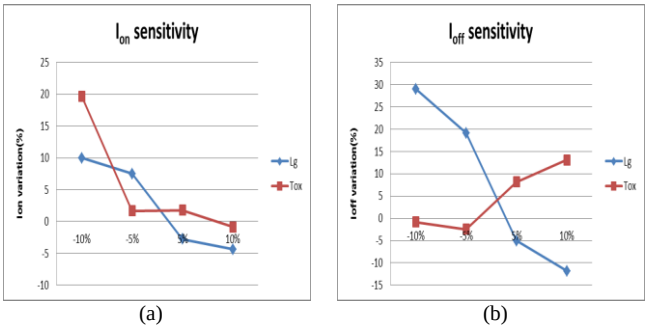
Fig. 6. (a) DIBL sensitivity (b) Subthreshold slope sensitivity with variation of fin width and fin height.

### C. *Influence of Gate Length and Gate Oxide Thickness:*

The variation in gate length and gate oxide thickness have a large impact on leakage currents as seen in Fig. 7. A 10% increase in oxide thickness increases the subthreshold leakage current by nearly 15% while a 10% decrease in $T_{ox}$ leads to a large increase in gateleakage current. When $T_{ox}$ reduces by 10% from the nominal 1.2 nm to 1.08 nm, Gate leakage increases from 0.4 nA to 3.1nA leading to a increase in static power dissipation when the N FinFET is on. The On current also varies by a factor of nearly 20% with a 10% decrease in gate length. DIBL is especially sensitive to $T_{ox}$ variation while the subthreshold slope remains largely unaffected as seen in Fig. 8.

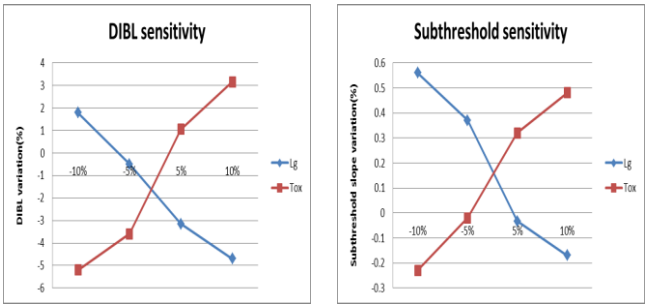
## IV. Comparison of Device Characteristics

The Gate input capacitance calculated using C-V curves is 0.271fF. Therefore, a constant lumped capacitance of 0.813fF (due to loading of the next stage, $C_L$=3×$Cgg$) is connected to the output of the inverter.




(a) (b)

Fig. 7. (a) $I_{on}$ sensitivity (b) $I_{off}$ sensitivity with variation of Gate length and gate oxide thickness.




(a) (b)

Fig. 8. (a) DIBL sensitivity (b) Subthreshold slope sensitivity with variation of gate length and gate oxide thickness.

### A. *Power Dissipation and Delay:*

The main leakage components in a transistor when it is off are the sub threshold leakage $I_{sub}$,, Gate leakage $I_{gd}$, and the band-to-band tunneling leakage $I_{btbt}$. When the transistor is on, the main leakage component is the gate leakage, $I_{gd}$. The Static power dissipation is given by

$$P_{static} = (I_{sub} + I_{gd} + I_{btbt})\, V_{dd}. \quad (1)$$

Table II gives the total power dissipation and delay for Inverter with SOI FinFETs and it is compared with that of UTB SGOI recessed source drain MOSFETs. It is shown that inverters with SOI FinFETs have reduced subthreshold leakage as well as gate leakage and hence static power dissipation is considerably reduced making them suitable for LSTP applications. However, rise time delay increases by 45.7% while the fall time delay reduces by 100% in these gates.

TABLE II: Power Dissipation and Delay in Inverter

| | Static Power dissipation | Delay | | Dynamic Power Dissipation (fW/Hz) |
|---|---|---|---|---|
| | | Rise time | Fall time | |
| UTB SGOI Recessed source drain MOSFET [14] | 269.8nW | 3.79p | 1.475p | 3.6 |
| SOI FinFET | 0.449nW | 6.98p | 0.733p | 0.788 |

The Gate delay for the inverter is given by

$$\tau = C_L \times V_{dd}/I_{on}. \quad (2)$$

The Dynamic Power Dissipation per unit bandwidth is given by

$$P_{dynamic}/\,Hz = C_L \times V_{dd}^2 \quad (3)$$

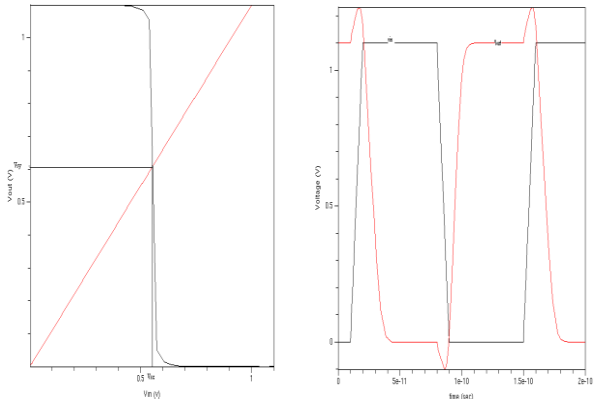
### B. *Noise Margin:*

The Noise Margins for the inverter are obtained from the

voltage transfer curves seen in Fig. 9 and are given by

$$NM_H=V_{OH}-V_{Sx} \quad (4)$$

$$NM_L=V_{Sy}-V_{OL} \quad (5)$$



(a) (b)

Fig. 9. (a)Voltage transfer characteristics of CMOS inverter (b) Inverter transient response.

The values of the $NM_H$ and $NM_L$ are 0.55 and 0.6 respectively for SOI FinFET Transistors and 0.57 and 0.58 respectively for UTB SGOI recessed source drain MOSFETs.

## V. Conclusion

SOI FinFET electrical performance is much better compared to that of UTB Recessed Source drain SGOI MOSFET in terms of Subthreshold leakage and gate leakage currents. Also, the SCEs such as DIBL is improved. The influence of process parameters such as gate length, Oxide thickness, Fin dimensions and Fin doping on the device performance has been reported. The Fin doping is not required as the SCEs are well controlled in SOI FinFET structures thus minimizing the variations due to random dopant fluctuations. The gate leakage current which is a predominant source of static power dissipation in on state devices is much reduced in SOI FinFETs due to thicker gate oxides thus making the FinFETs more suitable for low standby power applications.

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