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Experimental Studies on Class E Inverter based Induction Heater

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Abstract—**This paper presents simulation and implementation of class E inverter based induction heater system. DC power is converted into high frequency AC power using class E inverter. This high frequency AC is used for induction heating. Open and closed loop systems are modeled and they are simulated using Matlab Simulink.The results of simulation and implementation are presented.The Experimental results are compared with the simulation results.**

I. Introduction

IN the high-efficiency Class-E power amplifier, the transistor is used as a switch. The resonator L_0, C_0 is used to block the harmonic frequencies and DC component, forcing the output current I_0 to approximate a sine wave at the fundamental frequency, with harmonic content as discussed in [10]. The radio frequency choke L_{RF} is assumed to be ideal such that it conducts only the DC current. The current into switch S and capacitor C_s must be a DC -offset sine wave, with some harmonic content as discussed in [10]. By appropriately adjusting the amplitude and phase of the load current, a solution is found with zero capacitor charge just prior to turn-on.

This results in a switching waveform with zero voltage and zero voltage slopes at turn-on. The conditions are those of the well-known Class-E switching [2], [16], [18]. This allows high-efficiency operation at frequencies up to 10 GHz,. Additionally, the Class-E topology can be implemented with fewer components because the

Power MOSFETs' parasitic capacitors can be incorporated into the circuit. These benefits have allowed the Class-E topology to achieve high power density, thus reducing the size and weight of the equipment. However, a blocking filter L_0, C_0 is needed to block the harmonic frequencies the shrinking size of electronic equipment demands ever-increasing power densities at high switching frequencies and a minimal parts count for the circuit technology [10][14]attempt to minimize the parts count with Class-E operation, the one-inductor one-capacitor Class-E high-efficiency switching-mode tuned PA [1] provides a more simplified circuit. this simplified single-ended circuit is appropriate only for applications in which the harmonic content and the phase-modulation noise of the output are not important criteria. It is therefore desirable to retain the functions of the conventional Class-E features; i.e., that the amplifier can be operated with high efficiency at very high frequencies and provides a sinusoidal output waveform and power-handling capability without increasing the complexity of the power circuits [17] [18].The proposed push–pull Class-E amplifier and the conventional single-ended circuit configuration that includes one inductor and one capacitor. As expected, the harmonic contents of output voltage are significantly reduced in the proposed push–pull amplifier. However, the amplitudes of the positive and negative half-cycle in the output-voltage waveform are not symmetrical, which may cause a small second-harmonic component, there is the additional benefit that the even harmonics are suppressed at the load.

Inductors and capacitors are not identical, Because of their nonlinearity and that the tolerance of the component characteristics differ appreciably. The approaches presented here can be applied to the analysis and design of other Class-E amplifier configurations or with more complicated circuits in exact designs. Further, it should be noted that for this topology, the circuit described in this paper has two operational points that are performed by the ZVZS and ZVZC switching. Unlike the single-ended Class-E amplifier [11 [12] the pushpul architecture is able to achieve a sinusoidal output waveform and high power-handing capability. For instance, a symmetrically driven push–pull Class-E amplifier has been proposed for high-power applications as shown in Fig.1.

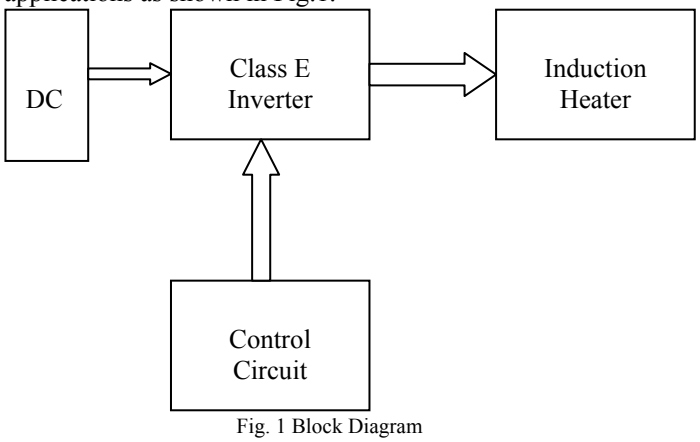

Fig. 1 Block Diagram

With the symmetrical gate-driving signals, theoretically, the even harmonics are entirely cancelled at the load, and thus there are fewer harmonic distortions (HDs). However, this doubled parts-count configuration incurs penalties on the overall efficiency and the design cost. Recently, the Class-E/F [16] and the current-mode Class-D [17], with low peak voltage and/or low rms current, have been implemented

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as a high-frequency amplifier, However, the current-mode Class-D and the Class-E/F only achieve zero-voltage switching (ZVS) conditions. Fortunately, there is a more elegant way to further reduce the switching loss, if the switch current increase gradually from zero after the switch is closed. This paper suggests a push–pull Class-E resonant PA with a simple LC load network and a load resistor R_L in each half-amplifier[8][9], overlapped capacitor-voltage waveform is utilized to achieve the nominal Class-E conditions without increasing the complexity of the power circuits. For nominal operation, the following performance parameters are determined: the current and voltage waveforms, the peak values of drain current and drain-to-source voltage, the output power, the power-output capability, and the component values of the load network [18].

II. Principle of Operation

The basic schematic of the proposed push–pull Class-E series- parallel LCR resonant PA is shown in Fig. 2. It contains two MOSFETs, two inductors, two capacitors, and a load resistance.

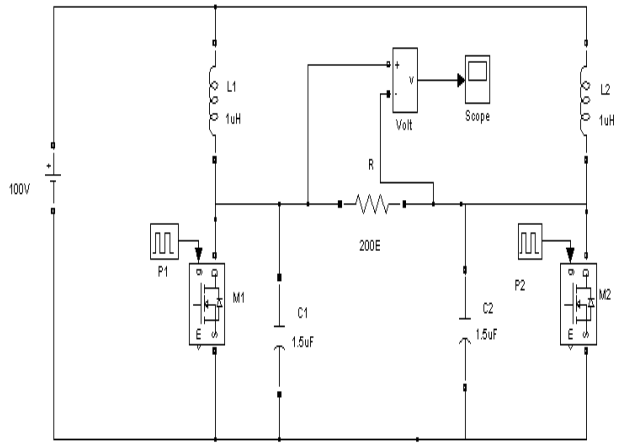

Fig 2.b.Proposed Simulation model

Switches S1 and S2 are complementarily activated to drive periodically at the operating frequency f = ω/2Π as in a push–pull switching PA [27], i.e., the switch waveforms are identical, except that the phase shifts between S1 and S2 are Π with an "on" duty ratio D of less than 50%. The simplest type of half-amplifier, as shown in Fig. 1(d), is a series-parallel resonant circuit, which consists of an inductor L in series with a paralleled capacitor C and resistor R. The resistor R_L is the load to which the AC power is to be delivered, with neither end connected to a ground. It is suitable for a load that is balanced to a ground, but most RF-power loads have one end connected to a ground.

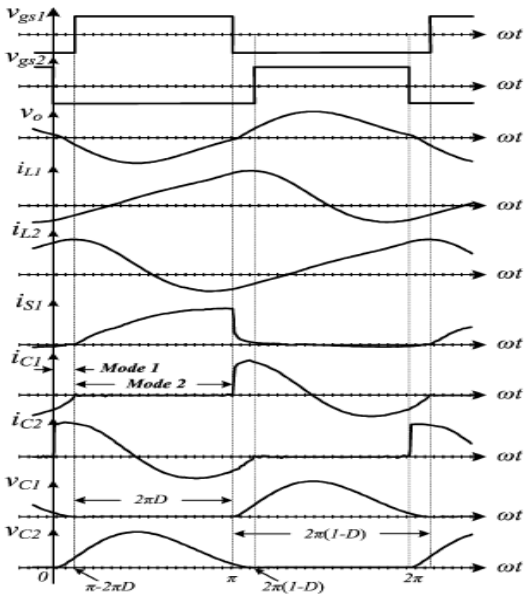

Fig.3.Theoretical Waveform

To accommodate grounded loads, the proposed topology needs to add one of the following: a balun that can be used to provide the interface with the amplifier or a two-winding transformer (that has V_i connected to a center-tap on the primary winding), between the grounded load (on the grounded secondary winding) and the drains of S1 and S2 (connected to the ends of the center-tapped primary winding). The switching sequences and theoretical waveforms for the steady-state operation of the proposed amplifier are illustrated in Fig. 3. To reduce the transistor turn-on power losses, the switch current i_s increase gradually from zero after the switch is closed. The proposed push–pull Class-E PA uses a pair of LC resonant networks with an overlapped capacitor-voltage waveform; this offers additional degrees of freedom, and thus there are two operational points that can validly achieve this situation:

Case 1) [Zero-Voltage Zero-Slope Switching (ZVZSS)]: In this case, the nominal operating conditions of ZVS and zero-voltage-slope switching (ZVSS) are simultaneously satisfied. Namely

$$\begin{cases} \upsilon_{C1}(\pi\text{-}2\,\pi D) = 0 \quad \text{---------- (1)} \\ \dfrac{d\upsilon C1(\pi\text{-}2\,\pi D)}{dt} = 0 \text{ --------- (2)} \end{cases}$$

Case 2) [Zero-Voltage Zero-Current Switching (ZVZCS)]:

The operation principle in the commutation of this case is solved by the following simultaneous equations:

$$\begin{cases} \upsilon_{C1}(\pi\text{-}2\pi D) = 0 \\ i_{L1}(\pi\text{-}2\pi D) = \dfrac{-\upsilon_{C2}(\pi\text{-}2\pi D)}{R_L} \quad \text{---- (3)} \end{cases}$$

In order to satisfy both case 1 and case 2, it is necessary to find the current $i_{L1} = -i_{RL}$ by which the switch current increases gradually from zero at time t = (Π – 2ΠD)/ω, as

shown in Figs. 2 and 3. The duty ratio must be kept at less than 50% so that the capacitor-voltage waveforms $V_{C1}$and V_{c2} can be overlapped.

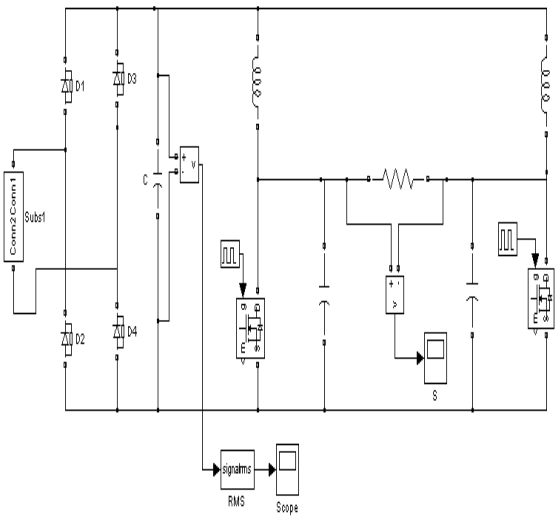

Fig.4a. Matlab Simulation circuit

III. Simulation Results

Class E inverter system is simulated using simulink and the results are given here. Fig.4a. Matlab Simulation circuit Class E inverter circuit is shown in Fig 4a. DC input voltage is shown in Fig 4b. Driving pulses are shown in Fig 4c. The pulse given to the second switch is shifted by 180 Degree with respect to the pulse of Switch 1.Voltage across M1 is shown in Fig 4b. Voltage across M2 is shown in Fig 4e.Voltage across the inverter is shown in Fig 4f.It can be seen that the output voltage is almost sine wave and the spectrum for the output is shown in Fig 4g. The THD value is 3.3%.

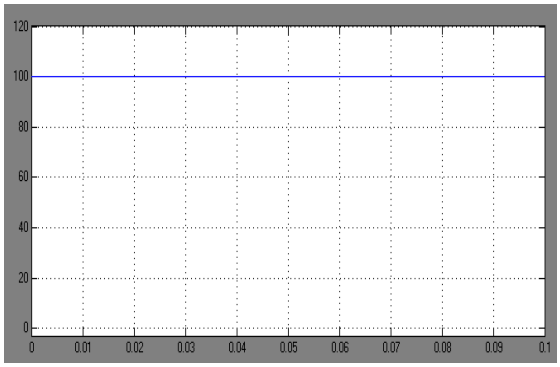

Fig.4.b. DC input voltage

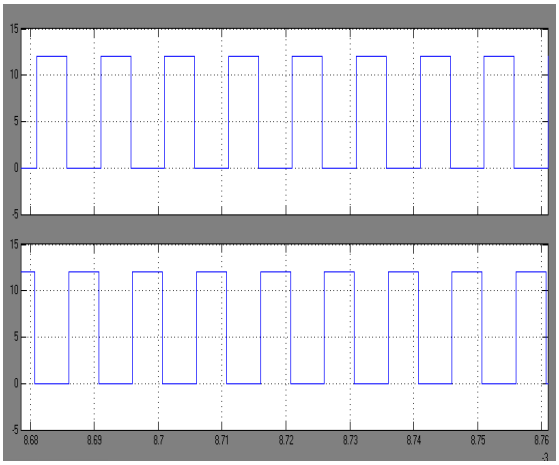

Fig.4.c.Driving pulses

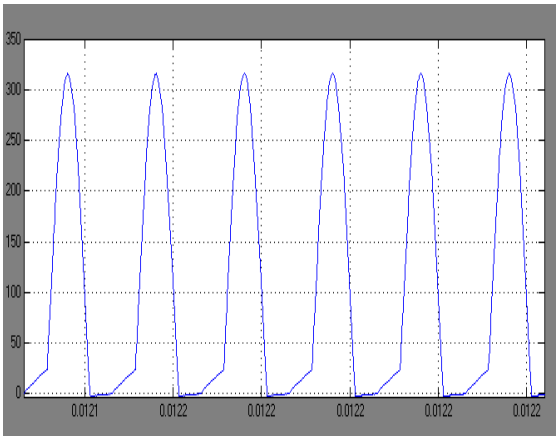

Fig 4.d voltage across switch 1

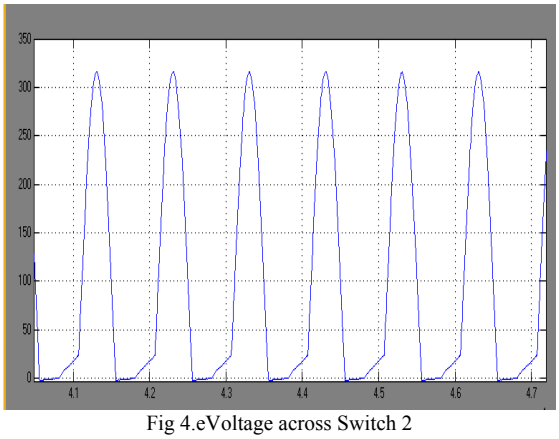

Fig 4.eVoltage across Switch 2

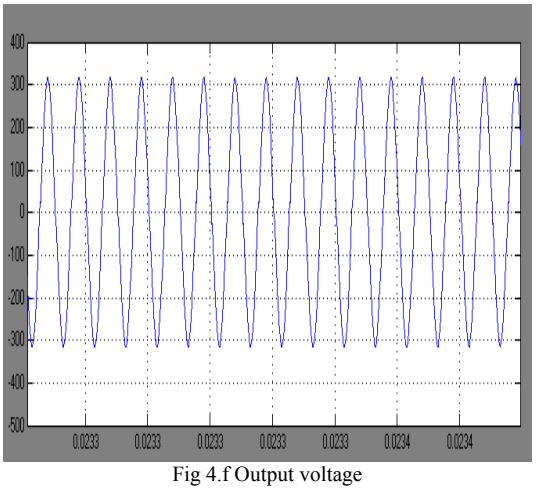

Fig 4.f Output voltage

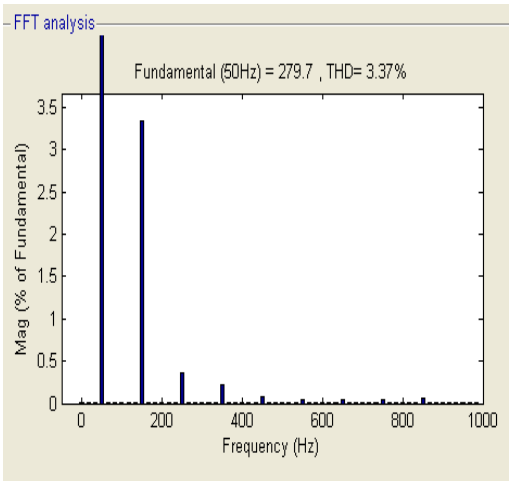

Fig 4.g FFT Analysis for output voltage

IV. Experimental Results

The laboratory model for class E inverter fed induction heater is fabricated and tested. Top view of the hardware is shown in Fig 5a. The hardware consists of power circuit and control circuit .Driving pulses for S1 and S2 are shown in Fig5b.Voltage across the MOSFET is shown in Fig 5c.Output voltage of the inverter is shown in Fig 5d.The output is not a pure sine wave due to the resistance of the coil.

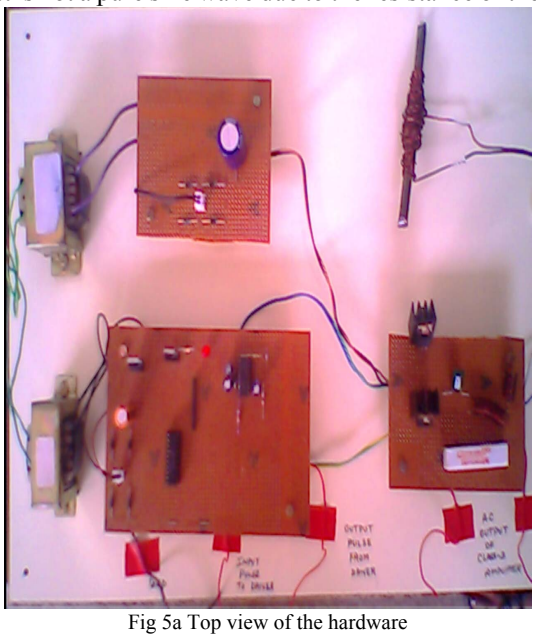

Fig 5a Top view of the hardware

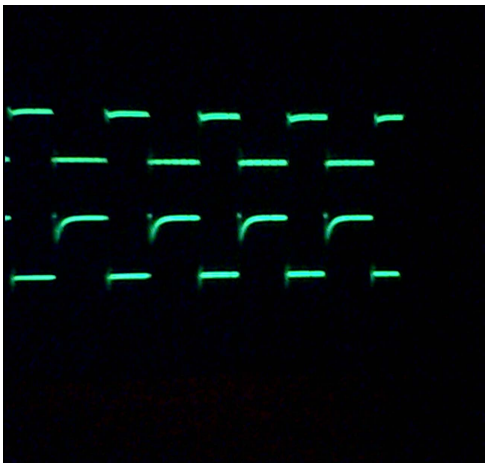

Fig. 5b Driving pulses for S1 & S2

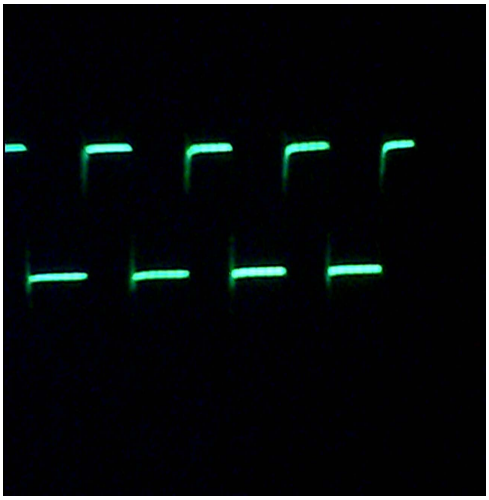

Fig.5c Voltage across switch1

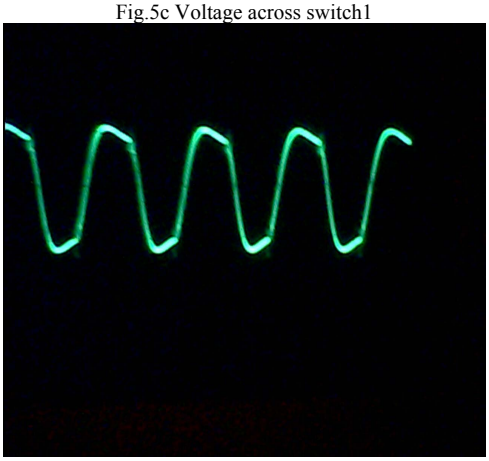

Fig.5d Output voltage

V. Conclusion

This work has presented simulation and implementation of class E inverter based induction heater system. This system has advantages like low switching losses, reduced stress and increased power density. The hardware as fabricated and tested. The experimental results are in line with the simulation results. This inverter system can also be used for dielectric heating.

The output voltage is not a pure sine wave due to the presence of load resistance. The scope of this work is the simulation and implementation of open loop system. The closed loop hardware is yet to be completed.

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