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Study and Simulation of Fault Tolerant Quantum Cellular Automata Structures

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***Abstract*—Quantum cellular automata (QCA) is a new technology in nanometer scale as one of the alternatives to nano cmos technology, QCA technology has large potential in terms of high space density and power dissipation with the development of faster computers with lower power consumption. This paper proposes Fault tolerant Quantum cellular elementary Block type QCA logic gates and analysis its polarization values. The simulation is carried out using QCA designer tool and it was found that maximum displacement of 34 nm for QCA input cells and 8 nm for QCA output cells of fault tolerant logic gate gives same results as that of the ordinary QCA logic gates. Further this analysis can be carried out for displacement of electron dots within the cells and study other device level parameters like radius of interaction cells, clocking zones of the cells, no of cell displacement in a clock zone and electron migration etc. Fault tolerance analysis applied here can be used to find the defective cell from its polarization value.**

***Index Terms*—Quantum Cellular Automata circuits (QCA), Fault tolerant gates, Polarization, Majority Voting and Displacement faults.**

I. Introduction

The Quantum cellular automata (QCA) have been one of the promising nanotechnologies of the future. The analysis and simulation of the QCA circuits has many challenges. QCA circuit simulation involves larger computational complexity. Quantum dots are nanostructures created from standard semi conductive materials. These structures are modeled as quantum wells. They exhibit energy effects even at distances several hundred times larger than the material system lattice constant. A dot can be visualized as well. Once electrons are trapped inside the dot, it requires higher energy for electron to escape. Quantum dot cellular automata is an Novel technology that attempts to create general computational functionality at the nanoscale by controlling the position of single electrons [1][2][8]. The fundamental unit of QCA is QCA cell created with four quantum Dots positioned at the vertices of a square.[1] [8]. The electrons are quantum mechanical particles, they are able to tunnel between the dots in a cell. The electrons in the cell that are placed adjacent to each other will interact; as a result the polarization of one cell will be directly affected by the polarization of its neighboring cells.

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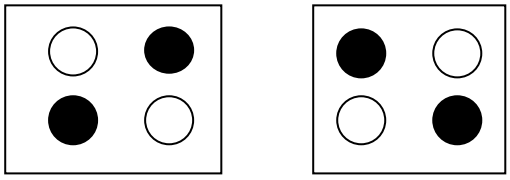

1(a) 1(b)

Fig 1 QCA cells with four quantum dots.1 (a) P = +1 (Binary 1) 1(b) P = -1 (Binary0) [1][2][4][8]

Fig 1 shows quantum cells with electrons occupying opposite vertices. This interaction forces between the neighboring cells able to synchronize their polarization. Therefore an array of QCA cells acts as wire and is able to transmit information from one end to another [5][6]. Thus the information is coded in terms of polarization of cell. Polarization of each cell depends on polarization of its neighboring cells. To perform logic computing, we require universally a complete logic set. We need a set of Boolean logic gates that can perform AND, OR, NOT and FANIN and FAN OUT [3] Operations. The combination of these is considered as universal because any general Boolean function can be implemented with the combination of these logic primitives. The fundamental method for computing is majority gate or majority voter method [1] [4]. Suppose three inputs are given to QCA circuit, then the output of the QCA structure is tabulated in table 1.

TABLE 1 Majority voting scheme [4] [5]

INPUT	OUTPUT MAJORITY VOTING
000	0
001	0
010	0
011	1
100	0
101	1
110	1
111	1

The majority gate produces an output that reflects the majority of the inputs. The majority function is a part of a larger group of functions called threshold functions.

Threshold functions works according to inputs that reaches certain threshold before output is asserted. The majority function is most fundamental logic gate in QCA circuits. In order to create an AND gate we simply fix one of the majority gate input to 0 (P = -1). To create OR gate we fix one of inputs to 1 P = +1. The inverter or NOT gate is also simple to implement using QCA. If we place two cells at 45 degrees

with respect to each other such that they interact inversely.

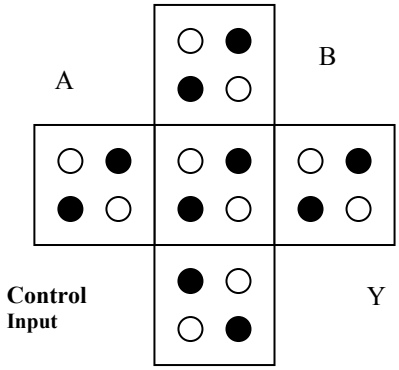

Fig 2.Majority AND gate [6] [11]

The output of majority AND gate reflects the majority of the inputs. Suppose input A =1, B = 1, Control input 0(-1), the output is equal to 1.

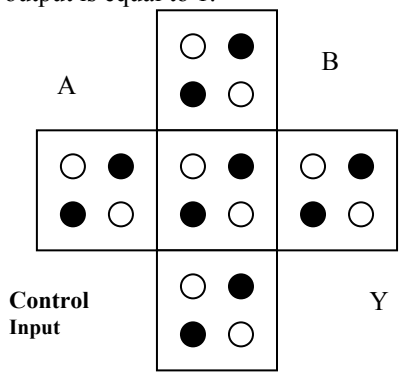

Fig 3 Majority OR gate [6][11][12]

Figure 2 and 3 shows the majority AND and OR gate structure. Control input to AND gate is -1 and for OR gate is +1.

Figure 4 clocking scheme of QCA circuits [4][5]

II. QCA Clocking

Clocking is the requirement for synchronization of information flow in QCA circuits. It requires a clock not only to synchronize and control information flow but clock actually provides power to run the circuit [9] [10] [11]. The cells are not powered from any other external source apart from the clock. These clocks have been proposed to control the potential barriers between the dots. When the clock signal is high the potential barriers between the dots are low and electrons effectively spread out in the cell and no net polarization exists. As the clock signal is switched low, the potential barriers between the dots are raised high and the electrons are localized such that a polarization is developed based on the interaction of their neighbors [7][12].. In order to pump information down a circuit in a controllable manner four clocking zones are available as shown in Figure 4. Each of clocking signal lagging in phase by 90 degrees with respect to one before.In this way, the cells are latched in series and propagate information in the same direction. So clocking is essential for QCA circuits. In this paper fault tolerance QCA circuits are proposed and the detailed analyses about tolerance circuits are discussed. All the circuits are simulated using QCADesigner tool.

III. Fault Tolerant QCA Gates

Two major categories of fault occur during the assembly of QCA circuits. First fault is due to displacement of cell from their intended location. The QCA cell displaced will be outside the radius of effect of its neighbour, So that no longer contributing to the interaction among the cells. A typical maximum distance at which interaction exists is 40 to 60nm. The interaction between the cells are due to electrostatic quadruple – quadruple interactions between adjacent cells of two free electron and two fixed proton in each cell. These forces decay or fall off as the 5^{th} power of its distance from that cell, so the radius of effect; distance from the cell will always remain relatively small [13].

A cell that is displaced may have a polarity opposite or same as that of the neighbour. These displaced cells have an impact on the effectiveness of QCA circuit and some time they can cause a circuit to cease its functioning as expected [14]. Figure 4 shows QCA majority gate with 5nm displacement.

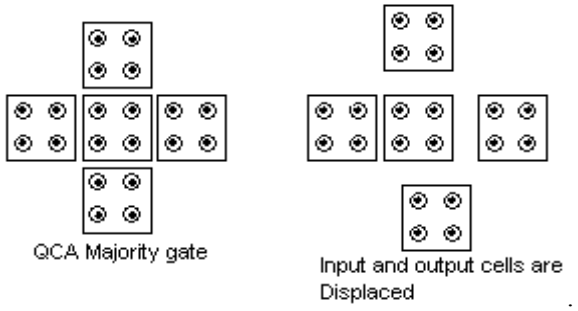

Figure 4 QCA majority gate, displaced input and output cell of 5nm

The second type of fault is due to defective nature of the cell itself. Defective cells will not interact in the same way as ideal cells. Here it is considered that the cell itself is missing and it has no influence on its neighbours. QCA circuits which are robust enough to function correctly in the presence of faults are very important. In this technology, the presence of smaller faults leads to more errors in terms of its interactions. So cell alignment at nanoscale level and manufacturing defects corresponds to greater relative defects. The only simplest way to avoid these faults is to design logic QCA circuit which gives output in the presence of some faults. Fijay and Toomain used fault version of majority voting gate [14] This gate uses array of quantum cells. The main goal is to design a gate that will work under limited no of potential defects. A fault tolerance gate should be robust enough to continue to operate correctly in the event so that one or more number of cells in the array are misaligned. A simple 5 X 5 Fault tolerant QCA tile latches, inverters and Majority gates are proposed. All the designs are tile based block circuits. These designs allow some defects to be cancelled out by other cells that are in correct state. The proposed design will work for limited number of faults.

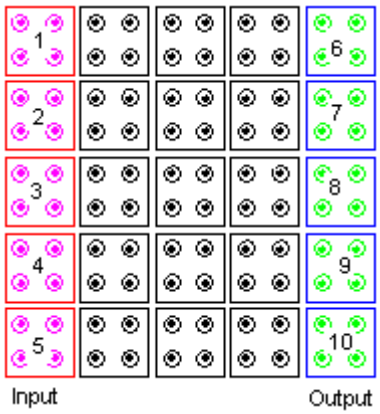

Figure 5 Tile based QCA latch

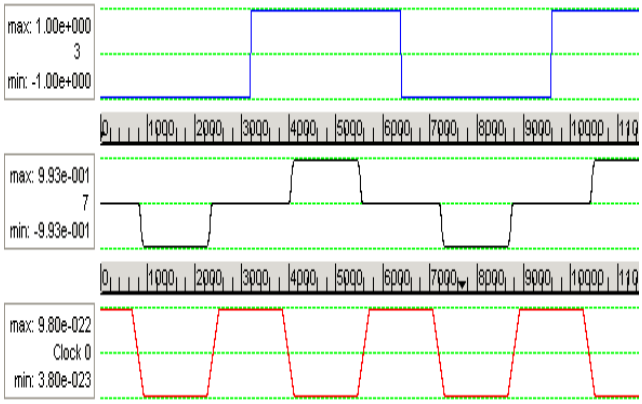

Figure 6 Simulated waveform of QCA latch

In figure 5 QCA latch of tile based design is constructed using QCA designer tool and figure 6 shows the simulated waveform of QCA latch. Table 2 shows polarization values of output cells 6 to 10 with given input cells 1 to 5.

TABLE 2 OUTPUT POLARIZATION OF QCA LATCH WHEN INPUT CELLS ARE ACTIVATED.

Output /input	**6**	**7**	**8**	**9**	**10**
1	**0.929**	**0.994**	**0.981**	**0.994**	**0.93**
2	**0.929**	**0.994**	**0.981**	**0.994**	**0.93**
3	**0.929**	**0.994**	**0.981**	**0.994**	**0.93**
4	**0.929**	**0.994**	**0.981**	**0.994**	**0.93**
5	**0.929**	**0.994**	**0.981**	**0.994**	**0.93**

The design has five possible output positions and five possible input positions. Simulations were run to determine the maximum output polarization for each of input –output combinations. The results are summarized in table 2. Simulation results show input position for Tile based design has no effect on the output results. Therefore five possible input cells are probably so close in polarization to each other. The best output position is 7 and 9, Input location of 3 with output location 7 and 9 are selected for analysis. QCAD Bistable approximation method is used for finding steady state polarization of the system. The energy of each cell is calculated by electrostatic energy between each and its neighbour cells. The energy of each cell is represented by equation 1.

$$E_{i,j} = \frac{1}{4\pi\varepsilon_o\varepsilon_r} \frac{q_i q_j}{|r_i - r_j|} \qquad (1)$$

The kink energy between two adjacent cells is defined as the difference in electron energy between two polarization states. The polarization of QCA cell is calculated as in [15].Each cell has a length of 18nm and quantum dot diameter of 5nm, the spacing between each cell is 2nm. The horizontal and vertical spacing between the dots in a cell is 9nm. The fault tolerant design being analyzed here has 25 cell and tile based circuit and the design relies on the majority voter like behavior of QCA cell and consists of paths for information to travel through the gate. Figure 7 shows the fault tolerant QCA NOT gate and Figure 7.1 is the fault tolerant QCA latch gate. Table 3 summarizes the range of movement for this design, some cells have no limitations for their movement in given direction indicated by 'inf' and other cells are restricted in movement by neighbor cells and their movement indicated by '-'.

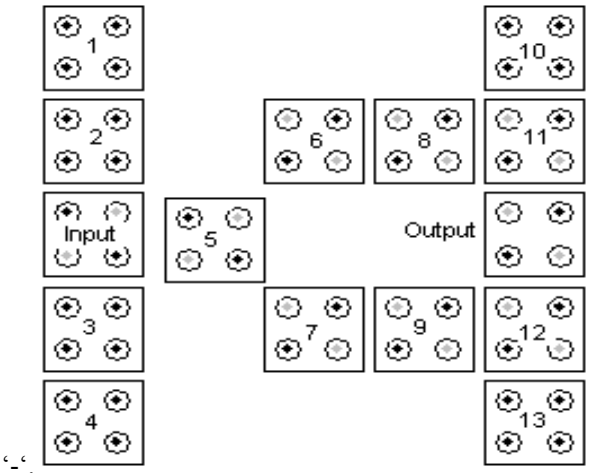

Figure 7 Fault tolerant QCA Not gate

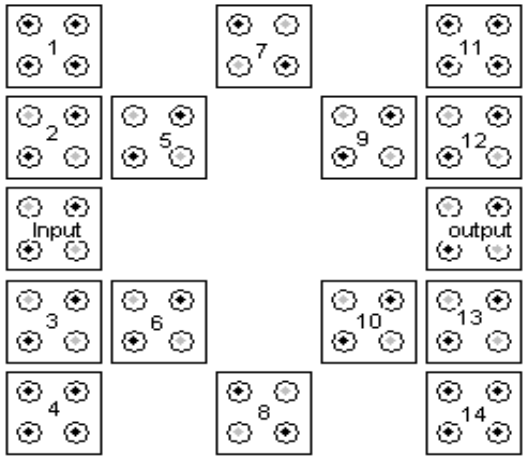

Figure 7.1 a Fault tolerant QCA Latch.

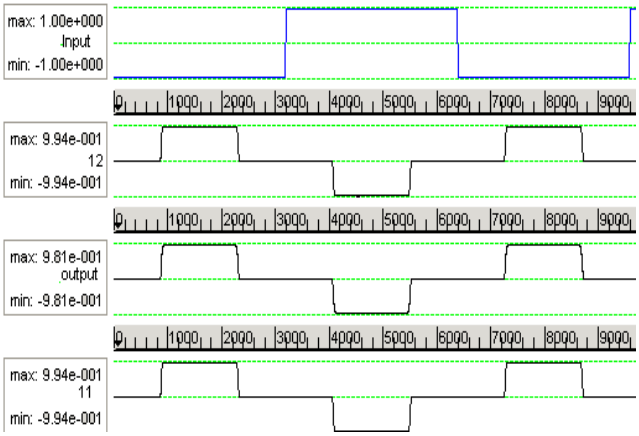

Figure 8 Simulated waveform of Fault tolerant QCA not gate.

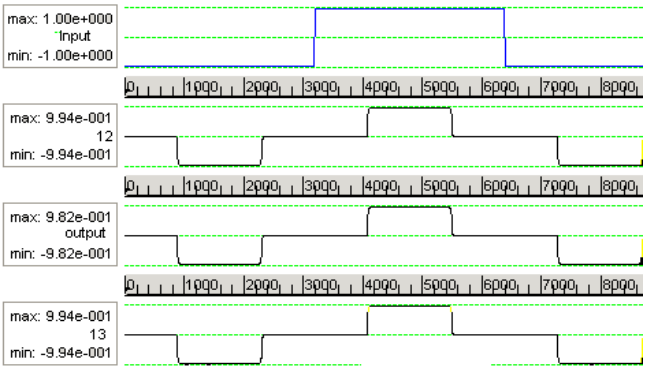

Figure 9 Simulated waveform of Fault tolerant QCA latch

TABLE 3 QCA LATCH DISPLACEMENT OF CELLS FOR FAULT TOLERANCE

Direction of movement	Up–'U'	Down – 'D'	Left – 'L'	Right -'R'
1	Inf	---	Inf	---
2	---	---	Inf	---
3	---	---	Inf	----
4	---	Inf	Inf	17 nm
5	Inf	Inf	----	Inf
6	Inf	Inf	---	Inf
7	8 nm	---	8 nm	8nm
8	---	----	8 nm	8nm
9	8 nm	8 nm	----	
10	8 nm	8 nm	----	----
11	Inf	----	17 nm	17 nm
12	----	----	17 nm	----
13	----	----	----	17 nm
14	---	8 nm	----	17 nm
Input	----	----	34 nm	17 nm
output	----	----	8 nm	17 nm

TABLE 4 QCA NOT GATE DISPLACEMENT OF CELLS FOR FAULT TOLERANCE.

Direction of movement	Up–'U'	Down – 'D'	Left – 'L'	Right -'R'
1	Inf	---	Inf	---
2	---	---	Inf	---
3	---	---	Inf	----
4	---	Inf	Inf	17 nm
5	----	----	----	---
6	----	----	8 nm	----
7	----	----	8 nm	----
8	8 nm	----	----	----
9	----	8 nm	----	----
10	Inf	----	17 nm	17 nm
11	----	----	----	17 nm
12	----	----	----	17 nm
13	----	Inf	8nm	17 nm
Input	----	----	34 nm	----
output	----	----	8 nm	17 nm

Analysis of the inverter and latch shows that this design is robust in presence of moderate displacement faults. In both the circuit the input cell can be shifted twice its size towards left side and output cell in inverter and latch can be shifted right side of maximum 17 nm, other cells displacement are shown in table 3 and 4. QCA not gate has 15 cells and latch circuit has 16 cells. The displacement faults are validated using QCAdesinger tool which gives same simulated results as in figure 8 and 9. Figure 10 shows the maximum displacement of cell in QCA not gate.

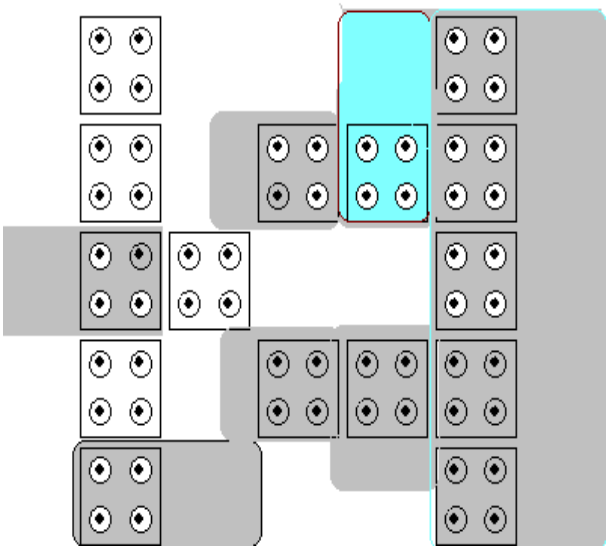

Figure 10 QCA Not shaded region shows maximum displacement of corresponding cell.

IV. QCA MAJORITY GATE

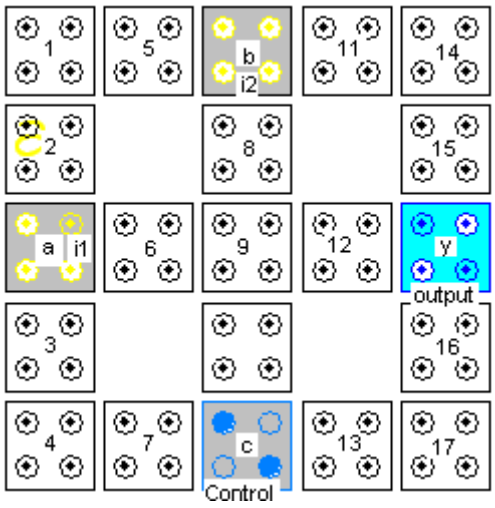

Figure 11 Tile based QCA Majority gate

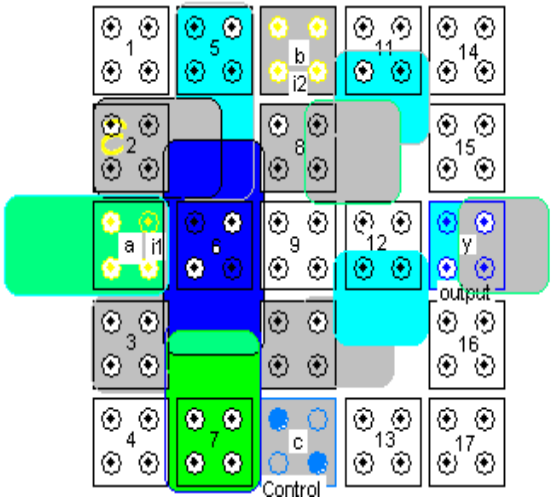

Figure 12 fault tolerant QCA majority gate

Tile based QCA Majority gate has 21 cells with three input and one output. Figure 11 shows QCA majority gate and Figure 12 is majority gates with their cells of maximum displacement without affecting the nearby cells. Table 5 shows the displacement of the cells with input cells of maximum displacement of up to 34nm and output cell of maximum 8 nm. The above table is verified using the simulation tool QCA designer from [15]. This fault tolerance gate gives same output as that of the ordinary majority gate. The same kind of analysis can be carried out for displacement of electron dots within the cells and other device level parameters like radius of interaction cells, clocking zones of the cells, no of cell displacement in a clock zone and electron migration etc. Fault tolerance analysis applied here can be used to find the defective cell from its polarization value.

TABLE 5 QCA MAJORITY GATE DISPLACEMENT OF CELLS FOR FAULT TOLERANCE

Direction of movement	Up–'U'	Down – 'D'	Left – 'L'	Right -'R'
1	inf	---	Inf	---
2	---	---	Inf	8nm
3	---	---	Inf	8nm
4	---	inf	---	----
5	inf	17nm	----	---
6	8nm	8nm	----	----
7	17nm	inf	----	----
8	----	----	8nm	8nm
9	----	----	----	----
10	----	----	8nm	8nm
11	inf	8nm	----	---
12	8nm	8nm	----	----
13	8nm	Inf	---	----
I1 input	----	----	34 nm	----
I2 input	Inf	---	----	----
Control	---	Inf	----	----
output	----	----	----	8 nm

V. CONLUSION:

Displacement fault tolerant circuit is proposed for tile based QCA circuits. The simulation results shows a maximum of 34 nm displacement for input QCA cell and 8 nm output QCA cell in majority and inverter circuits which gives same results as that of without displacement. This analysis is helpful to construct fault tolerant QCA circuits. The same kind of analysis can be carried for other types of defects like physical defects, absence of QCA cells etc.

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