

Network Performance Comparative Analysis of Torus and Modified Mesh Interconnections with Source Routing for Packet Loss

Ramesh B., Gururaj H. L., and Chandrika J.

Abstract—The network topologies performance can be measured by number of parameters such as throughput, latency and jitter. The performance degradation of a network will happen by a very crucial parameter called data loss. Transmission Control Protocol (TCP) is a widely deployed reliable transport protocol. Data Source routing, is a routing approach in which the path to the destination is determined by the source itself. Torus interconnect is a combination of regular ring and mesh topologies and it is widely used in parallel supercomputers. Torus interconnect reduces the number of hops to reach the destination and thereby it saves the energy. The paper evaluating the performance of Torus interconnection and modified mesh interconnect on the basis of packet loss with source routing using different traffic generation mechanisms for parallel transmissions and comparing the results. Results are drawn for various scenarios and analyzed which are useful for designing the interconnection networks.

Index Terms—Interconnection networks, modified mesh topology, packet loss, source routing, torus topology.

I. INTRODUCTION

In [1] paper, mainly attached different traffic agents to mesh interconnection topology, and also down the link only for 0.1 second when the first acknowledgement is going to receive by the sender. Evaluated three source-destination pairs and found that the performance of FTP mechanism is better than the constant bit rate mechanism for parallel transmission. Therefore FTP mechanism is most secure and reliable in Mesh interconnection with parallel transmission.

Torus interconnects is used for processing nodes in parallel system. [2] Torus based interconnection networks have been utilized extensively in the design of parallel computers in recent years. Torus topology is viewed as a mesh topology with nodes arranged in a rectilinear fashion of 2, 3 or more dimensions. The goal of computer architects is to increase the performance of their computer architectures. Fast circuitry, packaging technology, and parallelism increase the performance. The length of the link connecting a certain number of processors decreases when the density of processor package increases [3], [4].

In NoC implementation packet loss decreases the performance. Packet loss occurs when one or more packets of data traveling across a network fail to reach their destination [5], [6].

Various factors by which packet loss occurred are buffer overflow, congestion, corrupted packets rejected in-transit, faulty link, faulty nodes or deadlocks. Packet loss probability is also affected by down of links and distances between the transmitter and receiver [7].

In [8] paper, they had analyzed 2D Mesh performance by changing two parameters packet size and packet generation interval and found that the ratio of packet loss is constant in both cases where traffic generator with acknowledgement is not considered.

But when acknowledgement is considered in both cases, no packet loss has been found. So reliability can be achieved in a network with the traffic agent who uses acknowledgement mechanism. Due to the link down delay of transmission was found in the network.

In [9] paper, a new topology was proposed which reduces interconnections and links which results in lower power consumption by keeping the same level of reliability and performance compared to 2D mesh topology.

This paper implemented Torus interconnection topology and Modified Mesh topology with two different traffic agents with handshaking mechanisms using NS2. Simultaneously four source-destination pairs are communicating in simulation for the evaluation. Analysis has been done based on packet loss in different traffic.

Transmission Control protocol (TCP) is a widely deployed reliable network than User Datagram Protocol (UDP). Packet loss is more while using Constant Bit Rate (CBR) than File Transfer Protocol (FTP) of Application layer when implemented on basic network topologies.

The remainder of this paper is organized as follows. In Section II, related reviews are discussed. Section III, describes the system model of Torus interconnection network, which designed and implemented in NS2 and Section IV, evaluate the performance and shows the results of simulation. Finally, Section VI concludes this paper and defines topics for further research.

II. RELATED WORK

The numerous studies have done related to simulation on Torus and mesh topologies. Super computers of IBM uses five and six dimensional Torus interconnects. The two dimensional Torus interconnect nodes look like rectangular array of rows and columns and each node connected to its nearest neighbor. The NoC has been introduced as a new research area that emphasis on modeling and analyzing the on-chip interconnect. Sophisticated networks which have specialized switches and routers and absolute topologies are

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the main NoC points for analysis and optimization [10], [11]. Recently, many NoC architectures have been surveyed and compared for different performance metrics. In the paper [12], Torus interconnect is a combination of mesh interconnect and ring interconnect [13], [14]. NoC mesh interconnects topology was analyzed using NS-2 simulator

NS-2 is used to design the topology and generate different traffic using an exponential traffic generator [15]. Packets are sent at a fixed rate during active state, and no packets are sent during inactive state. Common network performance metrics such as drop probability, packet delay, throughput and communication load are analyzed against different buffer sizes and traffic injection rates using the traffic generators [15].

III. SYSTEM MODEL

The simulation interconnection architecture model consists of $m \times n$ mesh of switches. Switches consists a slot for a resource. A resource may be a processor core, a memory block, a custom hardware block or any other peripheral devices, which fits into the available slot and compiles with the interface with the network. Fig. 1 shows the architecture of Torus interconnection with 16 nodes.

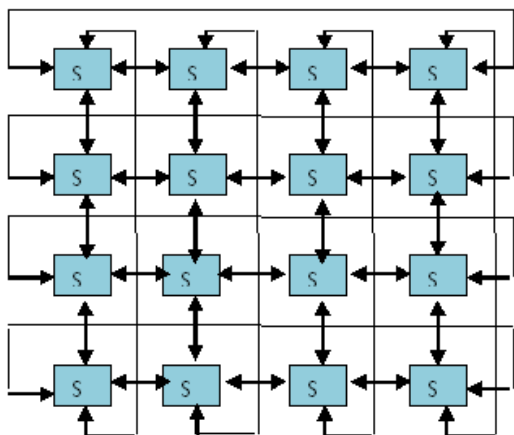


Fig. 1. 4 × 4 torus architecture.

A. Topology

A 4 × 4 two-dimensional Torus topology was designed and simulated using network simulator NS2. This topology is easily scaled to different sizes. Switch, resource and link are three basic elements in the topology.

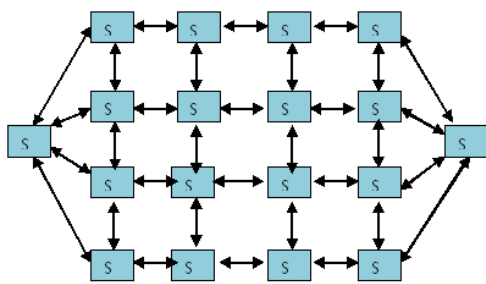


Fig. 2. Modified mesh architecture.

A 4 × 4 two-dimensional Mesh topology with two extra nodes was designed and simulated using network simulator

NS2. This topology is easily scaled to different sizes. Switch, resource and link are three basic elements in the topology. If N is total number of nodes in network. Number of links to connect these nodes in mesh = $N(N-1)/2$ each node should have $(N-1)$ I/O ports as it require connection to every another node. The Modified Mesh topology reduces the number of links in routing, thus resulting into lower power consumption keeping same level of reliability and performance level [16]-[18] (see Fig. 2).

B. Communication Links

Every node has a dedicated point to point link to every other node in the network. Each link carries traffic only between the two nodes it connects. The bandwidth and latency of the link is configurable. When any link down between two nodes it implies that the packet cannot be travel between these nodes in any direction. This assumption was drawn in [19] and is realistic, because bidirectional links are actually implemented by using a single wire.

C. Routing

An inter-communication path is composed of set of links identified by the routing strategy. A shortest communication path has been selected for each traffic pair before a simulation starts [3]. In both Torus interconnect and Modified Mesh topology routing decision will be takes at source node using source routing methodology [5].

IV. PERFORMANCE EVALUATION

In this section, to evaluate the performance of the Torus and Modified Mesh interconnection networks we develop a simulation model in NS2 with only built-in options. Tcl is used for specifying the Torus and Modified Mesh interconnection network simulation model and running the simulations. We have used existing routing algorithm to compute the path and for packet generation.

Our implementation of Torus and Modified Mesh interconnection networks uses the source routing to send packets from source node to destination node. In source routing the information about the whole path from the source to the destination is pre-computed and provided in packet header [4], [7].

In regular mesh topology the longest path a packet traverses is 6 hops, while in Modified Mesh topology the longest path a packet traverses is 5 hops as shown in the Fig. 4. In Modified Mesh topology a node(0) sends a packet to node(15) with 5 hops (node(0) → node(16) → node(12) → node(13) → node(14) → node(15)).

In Torus topology separate links are connected to edge nodes by which it reduces the number of hops while sending packet between those nodes. Node (0) sends a packet to node (15) just by two hops (node (0) → node (3) → node (15)).

The additional challenge with larger networks is scalability; it means the ability to add nodes without affecting performance and reliability of the system.

A. Simulation Environment

For the evaluation, a detailed event-driven simulator has been developed. This simulator models a 16-node 2-D Torus (4 × 4) and Modified Mesh (4 × 4) in which routing decision

will be takes at source node using source routing methodology. Each node is connected with point-to-point bidirectional serial links. The bandwidth of link is set to 1 Mb and latency/delay is set to the 10 ms. All these topology parameters can be describe as a script file in Tcl, as shown below:

```
#Default Values for topology:
set n 16;          # Total number of nodes
set max_bw 1Mb;  # maximum link band width
set linkDelay 10ms; # delay on each link
set pkt_size 500; # packet size
#Configuration for links between the nodes in topology
duplex-link $node (i) $node (i+1) $max_bw $linkDelay DropTail
```

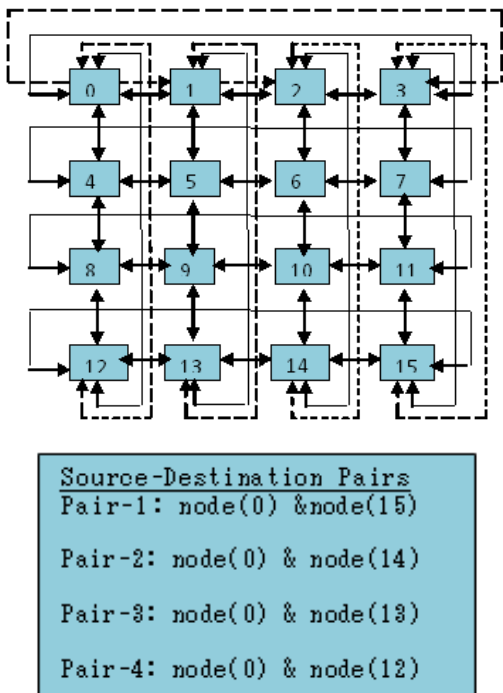


Fig. 3. Path and link in torus.

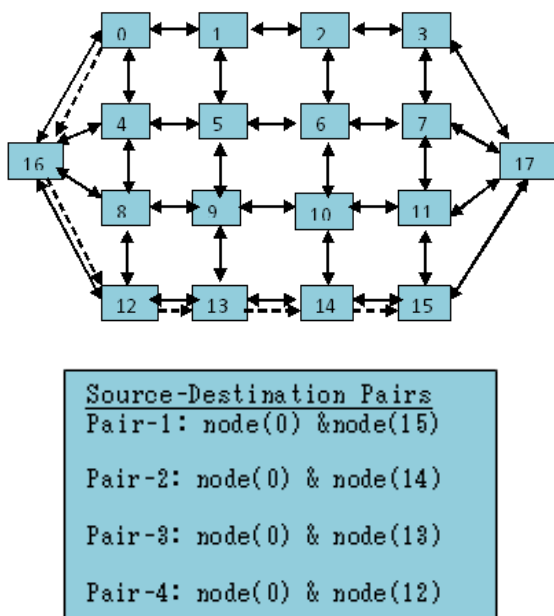


Fig. 4. Path and link in modified mesh.

In this environment, we fixed the source, destination node.

The time window of simulation is fixed 0.1 to 1.0 seconds.

In the simulation environment, the source and destination pairs are fixed, where pair-1: node (0) & node (15), pair-2: node (0) & node (14), and pair-3: node (0) & node (13), and pair-4: node (0) & node (12). Here model uses a common source node (0) for every pair. See Fig. 3 and Fig. 4, where dotted arrows show the path for each pair. The simulation time is fixed for 1second, where packet generation window is from 0.1 to 1.0 second.

Scenario-1 Packet generation using constant bit rate mechanism

In this experiment simulation model uses the packet generation of traffic in a constant rate where the packet size and interval of packet generation are fixed. The following Tcl code shows the traffic configuration setting for constant bit rate packet generation:

```
#Traffic Configuration: Constant bit rate traffic source set
cbr0 [new Application/Traffic/CBR]
$cbr0 set packet Size_ 500 $cbr0 set interval_ 0.0625
```

Scenario-2 Packet generation using file transfer protocol mechanism

In this scenario simulation model uses the packet generation of traffic using file transfer protocol (FTP) mechanism. FTP represents a bulk data transfer of large size where the packet size and interval of packet generation are fixed. The following Tcl code shows the traffic configuration setting for FTP packet generation:

```
#Traffic Configuration: File transfer protocol source set ftp0
[new Application/FTP]
$ftp0 set packet Size_ 500 $ftp0 set interval_ 0.0625
```

B. Result Analysis

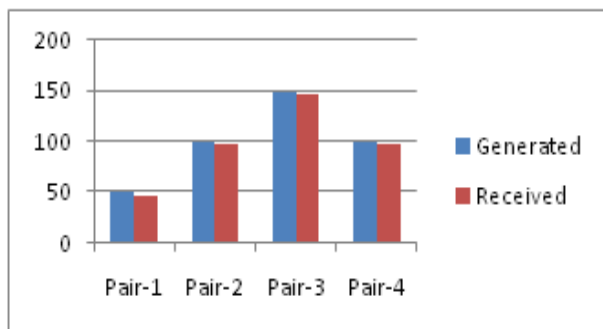
1) Parallel transmission using CBR traffic

In the first scenario Torus and Modified Mesh model uses the packet generation in a constant bit rate mechanism where the packet size and interval of packet generation are fixed. The source-destination pairs started the simulation for 0.1 seconds.

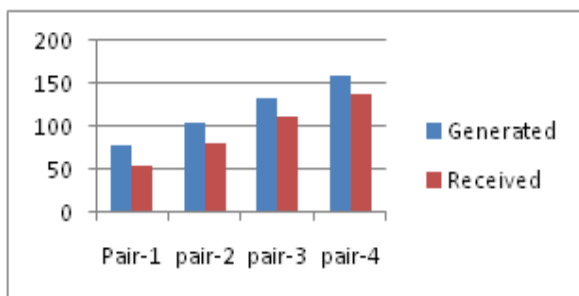
In Torus interconnect four parallel transmissions, results show that the total packet generated by source node is 51 packets and received by the destination node is only 47 packets in pair-1 and in pair-2, total 100 packets are generated by source and 97 are received by the destination and in pair-3, total 150 packets are generated by source and 147 are received by the destination and in pair-4, total 101 packets are generated by source and 97 are received by the destination. The generation of packets from source is decreases as well as some packets have been lost due to the link down for 0.1 second.

In Modified Mesh topology four parallel transmissions, results show that the total packet generated by source node is 78 packets and received by the destination node is only 54 packets in pair-1 and in pair-2, total 105 packets are generated by source and 81 are received by the destination and in pair-3, total 133 packets are generated by source and

111 are received by the destination and in pair-4, total 160 packets are generated by source and 139 are received by the destination. The generation of packets from source is decreases as well as some packets have been lost due to the link down for 0.1 second.



(a) Parallel communication in Torus interconnect



(b) Parallel communication in Modified Mesh interconnect

Fig. 5. Simulation graphs for constant bit rate transmission mechanism.

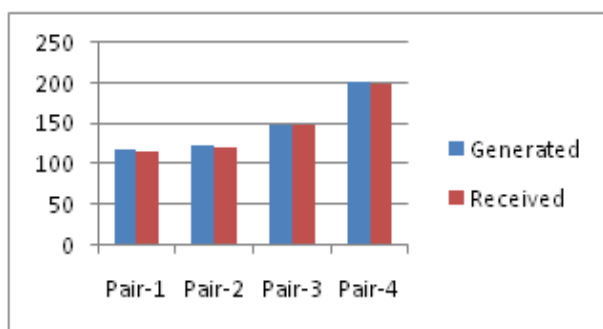
2) Parallel transmission using FTP traffic

In the second scenario Torus and Modified Mesh model uses the packet generation of traffic using file transfer protocol (FTP) mechanism. FTP represents a bulk data transfer of large size.

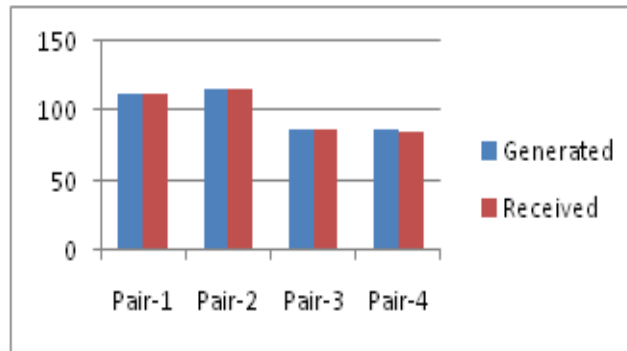
Like first scenario, made the pairs of the source, destination nodes and started the simulation for 1.0 seconds. After receiving the acknowledgement from each destination, source node sent the packets to destination node.

Using four parallel transmissions in Torus topology, pair-1 generates and receives total 118 packets, pair-2 generates and receives total 123 packets, pair-3 generates and receives total 149 packets and pair-4 generates and receives total 201 packets.

Using four parallel transmissions in Modified Mesh topology, pair-1 generates and receives total 113 packets, pair-2 generates and receives total 116 packets, pair-3 generates and receives total 87 packets and pair-4 generates and receives total 87 packets.



(a) Parallel communication in torus interconnect



(b) Parallel communication in Modified Mesh interconnect
Fig. 6. Simulation graphs file transfer protocol mechanism.

The parallel transmission using file transfer protocol mechanism is reliable and secure. It sends more data then constant bit rate mechanism and also no loss occurs. Number of packets sends is more in Torus topology as compared to Modified Mesh topology.

V. CONCLUSION

In the above experiments, 2D Torus and Modified Mesh interconnects of size 4×4 has been evaluated, and found that the performance of FTP mechanism is better than the constant bit rate mechanism for parallel transmission. Therefore FTP mechanism is most secure and reliable when parallel transmission is considered with handshaking concept in both Torus and Modified Mesh interconnection networks. Torus interconnects provides high performance as compared Modified Mesh topology as it traverse minimum number of hops to reach the destination. In future we are going to design a new topology which provides high performance and will analyze that topology using NoC standard benchmarks.

REFERENCES

- [1] L. Arora, "Performance evaluation of mesh with source routing for packet loss," *International Journal on Computer Science (IJCA)*, 2012.
- [2] Z. Ding, "Adaptive hybrid switching technique for parallel computing system," *International Journal on Computer Science (IJCA)*, 2000.
- [3] Direct interconnection networks I+II. [Online]. Available: <http://pages.cs.wisc.edu/~tvrdik/5/html/Section5.html>.
- [4] W. J. Dally and B. Towels, *Principles and Practices of Interconnection Networks*, Morgan Kaufmann Publishers, 2004.
- [5] A. Jantsch and H. Tenhunen, *Networks on Chip*, Kluwer Academic Publishers, 2003.
- [6] J. Flich, P. Lopez, M. P. Malumbres, and J. Duato, "Improving the performance of regular networks with source routing," in *Proc. the IEEE International Conference on Parallel Processing*, Aug. 2000, pp. 353-361.
- [7] M. Palesi, R. Holsmark, S. Kumar, and V. Catania, "Application specific routing algorithms for networks on chip," *IEEE Transactions on Parallel and Distributed Systems*, vol. 20, no. 3, March 2009.
- [8] G. Chiu, "The odd-even turn model for adaptive routing" *IEEE Transactions on Parallel and Distributed Systems*, vol. 11, no. 7, July 2000.
- [9] A. Patooghy and H. Sarbazi-Azad, "Performance comparison of partially adaptive routing algorithms," in *Proc. 20th International Conference on Advanced Information Networking and Applications*, vol. 2, 18-20 April, 2006.
- [10] M. Palesi, R. Holsmark, S. Kumar, and V. Catania, "A methodology for design of application specific deadlock-free routing algorithms for noc systems," *ACM Transactions*, Oct. 25-26, 2006
- [11] S. Kumar et al., "A network-on-chip architecture and design methodology," in *Proc. the International Symposium on VLSI (ISVLSI)*, 2002, pp. 117-124.
- [12] A. Hegedus, G. M. Maggio, and L. Kocarev, "A NS-2 simulator utilizing chaotic maps for network-on- chip traffic analysis," in *Proc.*

the IEEE International Symposium on Circuits and Systems (ISCAS), vol. 4, 2005, pp. 3375-3378.

- [13] L. Bononi and N. Concer, "Simulation and analysis of network-on-chip architectures: Ring, Spidergon, and 2D Mesh," in *Proc. Design, Automation and Test in Europe (DATE) Conference and Exhibition (Designers' Forum)*, 2006, pp. 154-159.
- [14] J. Xu, W. Wolf, J. Henkel, and S. Chakradhar, "A design methodology for application-specific networks-on-chip," *ACM Transactions on Embedded Computing Systems*, vol. 5, pp. 263-280, May 2006.
- [15] M. Moadeli, A. Shahrabi, W. Vanderbauwhede, and M. Ould-Khaoua, "An analytical performance model for the Spidergon NoC," *Advanced Information Networking and Applications*, 2007.
- [16] S. Suboh, M. Bakhouya, S. Lopez-Buedo, and T El-Ghazawi, "Simulation-based approach for evaluating on-chip interconnect architectures," in *Proc. SPL*, pp. 75-80, 2008.
- [17] L. Arora and R. Kumar, "Simulation and analysis of packet loss in mesh interconnection networks," in *Proc. on Development of Reliable Information Systems, Techniques and Related Issues*, Foundation of Computer Science, New York, USA, April 2012, pp. 35-38.
- [18] S. Mubeen, "Evaluation of source routing for mesh topology network on chip platforms," Master of Science Thesis, 2009.
- [19] M. Agarwal, "Comparative analysis of different topologies on network on chip architectures," *International Journal on Computer Science (IJCA)*, 2013.



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