

High Power and Low Phase Noise MMIC VCO Using 0.35 μ m GaN-on-Si HEMT

Hsuan-ling Kao, Bo-Wen Wang, Chih-Sheng Yeh, Cheng-Lin Cho, Bai-Hong Wei,
and Hsien-Chin Chiu

Abstract—A low phase noise and high power MMIC VCO using GaN-on-Si is presented. The VCO is based on common source series feedback to generate the negative resistance, using 0.35 μ m GaN HEMT on silicon substrate technology. The VCO can be tuned, between 3.92 GHz and 4.39 GHz, and has low phase noise, of -119 dBc/Hz, at a 1 MHz offset. The output power of the VCO is 14.5 dBm at 4.2 GHz from a 20 V power supply, while the total die size was 1.35 mm².

Index Terms—VCO, output power, phase noise, GaN HEMT, GaN-on-Si.

I. INTRODUCTION

Gallium Nitride (GaN) devices are of great interest because of their suitability for high power applications. AlGaN/GaN High Electron-Mobility Transistor (HEMT) technology has established itself as a strong contender for such applications, because of its large electron velocity ($>1 \times 10^7$ cm/s), bandgap (3.4 eV), breakdown voltage (>100 V) and sheet carrier concentration ($n_s > 1 \times 10^{13}$ cm⁻²). Most AlGaN-GaN HEMTs have been grown on sapphire [1]-[2], or SiC substrates [3]-[13]. The sapphire substrates are low-cost, but inefficient in heat dissipation, due to their poor thermal conductivity. GaN HEMTs on semi-insulating SiC have excellent crystal quality and thermal dissipation, due to reduced lattice mismatch and high thermal conductivity (4.9 W/cm \cdot K). The disadvantages of GaN-on-SiC are its higher cost and unstable crystal quality. Nowadays, there is increasing interest in growing AlGaN-GaN HEMT structure on Si substrate [14]-[20], which has the advantages of low cost, large-size substrate and good thermal conductivity (1.5W/cm \cdot K). The main challenge of GaN-on-Si is the cracking of GaN film due to stress. Recently, several authors presented studies on the power of AlGaN-GaN HEMTs on silicon substrate, at different frequencies [15]-[20]. The results, which demonstrate the capability to produce high power amplifiers and oscillators, make AlGaN-GaN HEMTs very attractive for future communication systems. The VCOs are also indispensable in fully integrated AlGaN/GaN HEMT transceivers. For GaN oscillators, some reports have presented the oscillators using GaN-on-SiC or GaN-on-sapphire in hybrid systems [1], [3]-[5], [14] or in monolithic microwave integrated circuit (MMIC) [6]-[13]. Only one has been reported a GaN-

on-Si power oscillator using hybrid system [14]. We proposed a 4.2 GHz 0.35 μ m GaN HEMT VCO based on the negative resistance concept using a common-source series feedback element. The VCO exhibits a frequency tuning range from 3.92 to 4.39 GHz with the varactor's voltage from -8 to 4 V. The phase noise of -119 dBc/Hz at 1MHz frequency offset at 4.2 GHz and output power of 14.5 dBm at a gate bias of -2.5 V and a drain bias of 20 V is achieved. The chip size is 1.5 \times 0.9 mm².

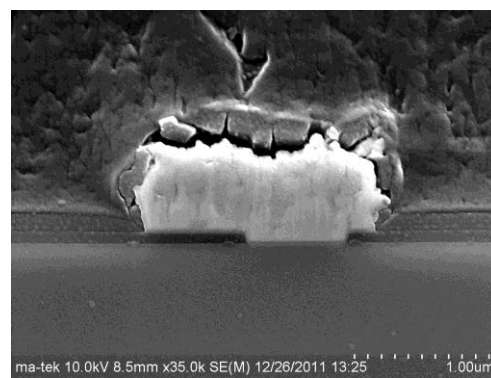
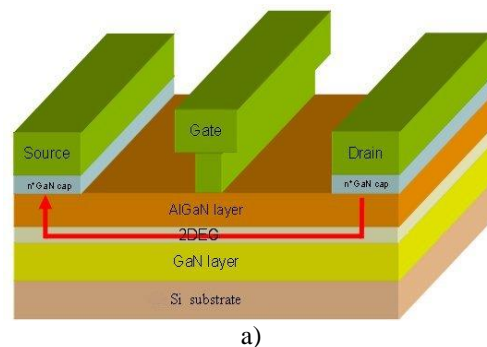


Fig. 1. The a) structure and b) SEM photograph of GaN HEMT.

II. DEVICE EPI-STRUCTURE AND PROCESS

Fig. 1 shows the schematic of GaN HEMTs structure. The devices used in this work were grown on silicon (111) substrate, using molecular beam epitaxy. The resistivity of the Si substrate was about $10^4 \Omega \cdot \text{cm}$. The epi-layer contained an AlN/GaN nucleation layer, a 1.8- μ m-thick layer of unintentionally doped GaN buffer, a 1-nm-thick AlN space layer, a 18-nm-thick Al_{0.27}Ga_{0.73}N barrier and a 1-nm-thick unintentionally doped GaN cap layer. Hall measurements confirmed a sheet-carrier density of 1.03×10^{13} cm⁻² and an electron mobility of 1,534 cm²/V \cdot s. Following mesa etching, ohmic contacts were prepared, using evaporated Ti-Al-Ni-Au multilayer metals, followed

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by annealing. A mushroom-shaped gate, based on Ni-Au metallization, is defined by a tri-layer resist scheme. The surface was passivated with SiO₂. The thickness of the silicon substrate was reduced to 100 μm, for better DC and RF power performance. All the HEMTs have a gate length of 0.35 μm. The HEMT devices display a maximum drain current density of 576 mA/mm and dc extrinsic transconductance (g_m) of 150 mS/mm. The unity current gain cutoff frequency (f_i) and maximum oscillation frequency (f_{max}) of the devices are 14.9 and 46.6 GHz. The maximum output power density of at 3.5 GHz is 1.58 W/mm ($V_{ds}=10$ V).

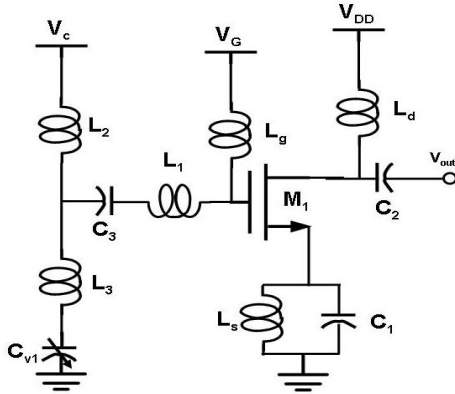


Fig. 2. Schematic of the ADS-designed 4.2 GHz VCO circuit which uses 0.35 m GaN HEMT on Si-substrate technology.

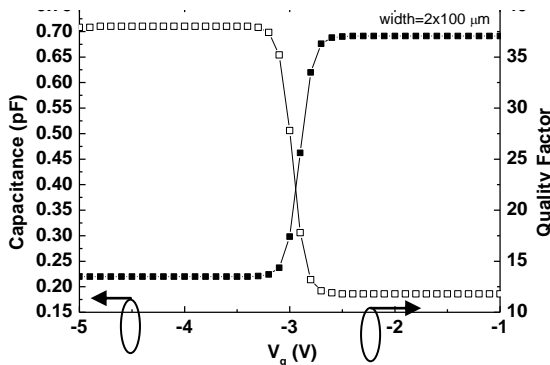


Fig. 3. The capacitance and Q-factor of varactors(Cv1).

III. DEVICE EPI-STRUCTURE AND PROCESS

This circuit uses a 0.35 μm GaN HEMT on Si-substrate process, provided by the foundry. The MMIC uses both airbridge to form a global interconnect layer and slot via under every source to achieve high gain and excellent thermal properties for circuit design. Fig. 2 shows the design of the 4.2 GHz VCO. The design is based on the negative resistance concept using a common-source series feedback topology. The VCO circuit is composed of M₁, C_{v1}, C₁~C₃, L_d, L_g, L_s and L₁~L₃. C_{v1} is the varactor of 2 × 100 μm width HEMT devices with the source-drain tied together as a two port network. The capacitance and Q-factor versus voltage are shown in Fig. 3. The operation bias of the varactor simulation is consistent with the VCO circuit in Fig. 2. The minimum capacitance is 0.22 pF, while the maximum capacitance is 0.69 pF. The width of M₁ is also 2×100 μm. L_s was connected between the M₁ source and ground, providing a positive feedback to make the transistor M₁

unstable. A shunt capacitor C₁ was in parallel with the L_s to shorten the stub's length and compact chip size. The LC tank, including L₁~L₃, L_g, C₃, C_{v1}, was connected to the gate of the M₁. C₃ is used also decoupled the negative gate bias and varactor's control voltage ($V_{control}$). C₂ is DC block capacitors. L_d is the DC feed inductor. GaN oscillators have large output signals without gain stage between core and load.

IV. DEVICE EPI-STRUCTURE AND PROCESS

The common-source series feedback VCO was simulated, using Advance Design System (ADS) software. Fig. 4 shows the layout of the fabricated VCO. Its size is 1.5 × 0.9 mm², including the probe pads. The 4.2 GHz VCO was tested on a wafer – the spectral density of the circuit being measured with a spectrum analyzer. The circuit is biased at $V_{ds}=20$ V, $I_{ds}=38$ mA, and $V_{gs}=-1.8$ V. The output spectrum of the proposed VCO is shown in Fig. 5. The center frequency is 4.2 GHz and output power is 14.5 dBm, including a 2.6 dB loss due to implementation. The rf-to-dc efficiency of the 4.2 GHz VCO is 3.8 %.

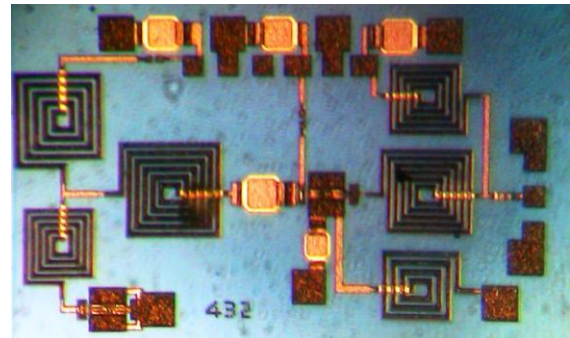


Fig. 4. Chip Image of a 4.2 GHz VCO circuit which uses 0.35 μm GaN HEMT on Si-substrate technology.

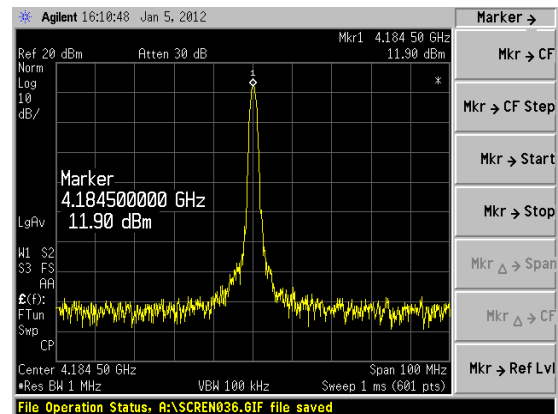


Fig. 5. The output power of a 4.2 GHz VCO circuit.

The output power of a 4.2 GHz VCO circuit which uses 0.35 μm Fig. 6 shows the phase noise, at 1 MHz offset, when operating at a controlled voltage of -4 V. The lowest phase noise is about -119 dBc/Hz, at 1 MHz offset from the 4.2 GHz carrier frequency. According to the Leeson formula [21]:

$$L(f_m) = 10 \log \left\{ \frac{1}{2} \left[1 + \frac{1}{f_m^2} \left(\frac{f_0}{2Q_L} \right)^2 \right] \frac{FkT}{P_s} \left(1 + \frac{f_c}{f_m} \right) \right\} \quad (1)$$

where $L(f_m)$ is single side band phase noise density, f_m is the

offset frequency, Q_L is the loaded quality factor, f_o is the resonant frequency, P_s is the amplifier's input signal power, F is its noise figure, k is the Boltzman constant, T is the temperature, f_c is the flicker corner frequency of the device.

It can be seen phase noise is inversely proportional to output power, so a large power is favorable from this point of view. Despite this, the demonstrated GaN-on-Si oscillator shows better phase noise compared to GaN-on-sapphire [2] or GaN-on-SiC [6]-[13].

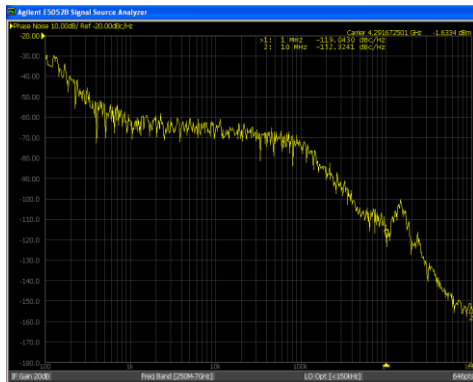


Fig. 6. The phase noise of a 4.2 GHz VCO circuit.

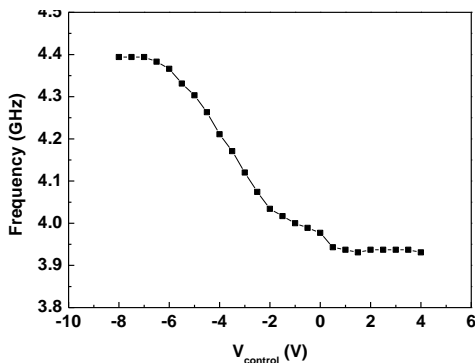


Fig. 7. The tuning range of a 4.2 GHz VCO circuit.

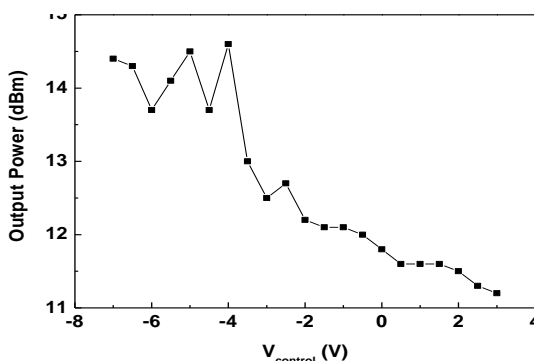


Fig. 8. The output power of a 4.2 GHz VCO circuit.

Fig. 7 shows the measured oscillation frequency of the VCO versus the controlled voltage ($V_{control}$) applied on the varactor. The proposed common-source series feedback VCO was tuned, from 3.92 GHz to 4.39 GHz, which is a tuning range of 468 MHz (near 11.4 % tuning range), with a tuning voltage varying from -8 to 4 V. The output power of the VCOs as a function of control voltage is shown in Fig. 8. Measured output power is 12.9 ± 1.7 dBm on a large frequency tuning range of 468 MHz. The maximum output power is 14.5 dBm at 4.2 GHz.

Table I summarizes the measured performance of the VCO and includes other reported performances, for the

purpose of comparison. Our differential VCO using GaN-on-Si technology achieved low phase noise and high output power, comparing well with, or better than, other published figures [6], [13], [22], [23].

TABLE I: SUMMARY OF MMIC OSCILLATOR FROM PREVIOUS STUDIES AND THAT OF THIS STUDY

Ref.	[6]	[13]	[22]	[23]	This Work
Process	0.7 m GaN HEMT on SiC	0.7 m GaN HEMT on SiC	0.09 m CMOS	0.18 m CMOS	0.35 m GaN HEMT on Si
f_o (GHz)	5	4.166	5.63	5	4.2
Tuning Range	single	33 kHz (0.7 %)	2.6GHz (45%)	390MHz (8.3%)	468 MHz (11.4 %)
Phase Noise (dBc/Hz)	-132@ 1MHz	-116@ 1MHz	-109@ 1MHz	-120@ 1MHz	-119@ 1MHz
P_{out} (dBm)	28.4 ~ 32.8	17.6~22.9	-9.88	2.2	14.5
Efficiency (%)	11~21.5	8.8	0.7	28	3.8

V. CONCLUSIONS

The fully integrated GaN HEMT VCO on Si-substrate demonstrated good circuit performance, in terms of high output power and low phase noise. The circuit was fabricated, using a 0.35 μ m GaN HEMT process. This 4.2 GHz VCO displayed a phase noise of -119 dBc /Hz, at a 1 MHz offset, and a 14.5 dBm output power while the total die size was 1.35 mm².

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