Development and Qualitative Analysis of a New Circuit Model of Two-Stage Small-Signal Sziklai Pair Amplifier

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***Abstract*—New circuit model of a two-stage small-signal Sziklai pair amplifier is proposed for the first time. The proposed amplifier circuit, which is obtained by cascading a small-signal Sziklai pair amplifier (Stage-1) with triple-transistor based compound Sziklai amplifier (Stage-2), is analyzed on the qualitative scale. Performance of the proposed amplifier is compared with that of Stage-1 and Stage-2 amplifier circuits to provide a wide spectrum to the qualitative studies. Proposed amplifier uses three additional biasing resistances in its circuit configuration and crops high voltage gain (237.50), high current gain (339.98) with wider bandwidth (2MHz) in 1-15mV range of AC input at 1 KHz. The proposed circuit successfully removes the poor response problem of conventional Darlington pair amplifiers at higher frequencies and narrow bandwidth problem of recently developed (by authors) circuit of small-signal Sziklai pair amplifier. Variation in voltage gain as a function of frequency and different biasing resistances, bandwidth and harmonic distortion of the amplifier is also pursued. The proposed amplifier may be useful for those applications where high voltage and current gain would be the prime requirement of amplification in a wider frequency range, spanned approximately from 200Hz to 2.5MHz.**

***Index Terms*—Small signal amplifiers, Sziklai amplifiers, complimentary Darlington pair amplifiers.**

I. Introduction

Single or multi-stage RC coupled Darlington pair amplifiers are popularly used to amplify small signals in the range of milli-volts [1]-[7]. These amplifiers are usually known for high β value but suffer from the problem of poor response at higher frequencies [3]-[6]. Researches and available literatures have widely explored the usefulness of Darlington pair amplifiers [1]-[7] but least efforts are made to configure a small-signal amplifier using Sziklai pair [8], [9], which is often compared with Darlington's unit due to almost identical value of β.

Sziklai pair [8], named after its inventor George Sziklai, is a composite unit of two bipolar transistors of opposite polarities (one NPN and other PNP transistor) and sometimes known as 'Complimentary Darlington pair'. Polarity of Sziklai pair unit is always determined by the *driver* transistor [8], [9].

The current gain factor (β) of Sziklai pair is slightly less than Darlington pair topology, because it has a small amount of in-built negative feedback which reduces the current gain [9]. However Sziklai pairs hold better linearity than Darlington pairs when used in linear circuits. Another major advantage of Sziklai pair over Darlington pair is that its base turn-on voltage is only half of the Darlington's turn-on voltage [8], [9].

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II. Experimental Circuits

Present paper crops a comparative study of small-signal Sziklai pair amplifier (Fig. 1), Compound Sziklai amplifier (Fig. 2) and a two stage proposed amplifier (Fig. 3), obtained by cascading circuits of Fig. 1 and Fig. 2 with minor modifications [10], [11].

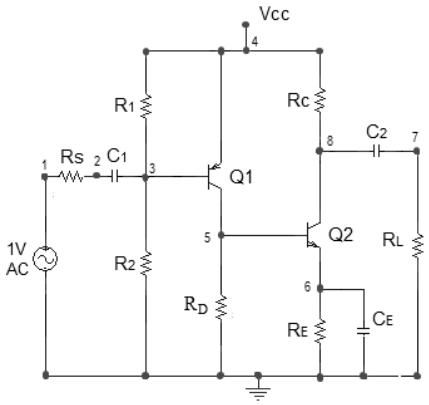

Fig. 1. Sziklai pair amplifier

Circuit of Sziklai pair amplifier [10] of Fig. 1 accommodates a PNP (Q2N2907A with β=231.7) driver-transistor Q1 and an NPN (Q2N2222 with β=255.9) follower-transistor Q2 in its paired unit. In addition, an extra biasing resistance R_D between collector of transistor Q1 and ground is introduced and emitter of PNP transistor Q1 is directly connected with the DC supply voltage. On the other hand, Compound Sziklai amplifier [11] of Fig. 2 is obtained by adding an extra PNP transistor Q3 and biasing resistance R_{D2} in the circuit of Fig. 1. Joint-unit of transistors Q1 (PNP) and Q2 (NPN) in circuit of Fig. 2 constitute PNP Sziklai pair while Q2 (NPN) and Q3 (PNP) jointly form Darlington pair like configuration.

However, the proposed two-stage Sziklai pair based small-signal amplifier, as depicted in Fig. 3, is obtained by cascading circuits of Fig. 1 and Fig. 2 with minor modifications. In this circuit (Fig. 3), emitter of the transistor Q1 of first stage Sziklai pair amplifier is connected to the collector of the transistor Q2 (at node-7 in Fig. 3) whereas in its original circuit it was directly connected to the V_{CC} (at node-4 in Fig. 1). The second stage of the proposed two-stage amplifier (Fig. 3) carries triple transistor based compound Sziklai amplifier after removal of biasing resistance R_1 from the original circuit (Fig. 2).

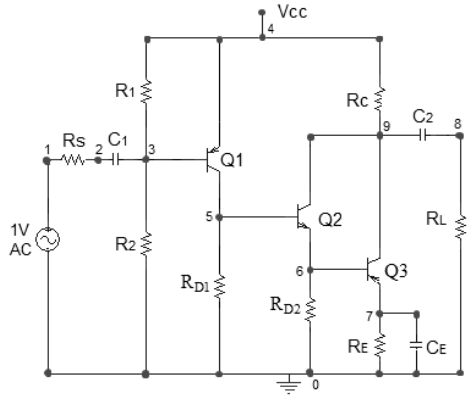

Fig. 2. Compound Sziklai amplifier

TABLE I: BIASING PARAMETERS AND CONFIGURATIONAL DETAILS

Components	Circuit of Fig.1	Circuit of Fig.2	Circuit of Fig.3
Q1	Q2N2907A	Q2N2907A	Q2N2907A
Q2	Q2N2222	Q2N2222	Q2N2222
Q3	Unavailable	Q2N2907A	Q2N2907A
Q4	Unavailable	Unavailable	Q2N2222
Q5	Unavailable	Unavailable	Q2N2907A
R_S	500Ω	100Ω	500Ω
R_1/R_{11}	33KΩ	33KΩ	33KΩ
R_2/R_{12}	100KΩ	100KΩ	47KΩ
R_{22}	Unavailable	Unavailable	100KΩ
R_C/R_{C1}	10KΩ	10KΩ	10KΩ
R_{C2}	Unavailable	Unavailable	10KΩ
R_E/R_{E1}	2KΩ	2KΩ	2KΩ
R_{E2}	Unavailable	Unavailable	2KΩ
R_{D1}	500Ω	500Ω	200Ω
R_{D2}	Unavailable	500Ω	500Ω
R_{D3}	Unavailable	Unavailable	500Ω
R_L	10KΩ	10KΩ	10KΩ
C_1 / C_2	1μF	1μF	10μF
C_3	Unavailable	Unavailable	0.1μF
C_{E1} / C_{E2}	0.1μF	0.1μF	0.1μF
Biasing Supply	+18V DC	+18V DC	+18V DC
Input AC Signal range for fair output	10-30mV (1KHz)	10-30mV (1KHz)	1-15mV (1KHz)

Biasing parameter and other details related to the configuration of all the amplifier circuits under discussion are listed in Table I. The first stage of the proposed two-stage amplifier (Fig.3) uses potential divider biasing methodology while the second stage uses fixed biasing methodology. All the observations mentioned in the present manuscript are furnished through PSpice simulation software [12] (Student version 9.2).

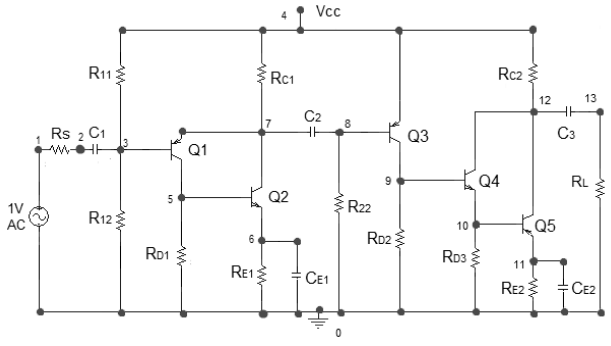

Fig. 3. Proposed two-stage amplifier based on Sziklai pair

Respective results are obtained by feeding the amplifier circuits with 1V AC input signal source from which, a small and distortion less AC signal of 10mV for Sziklai pair amplifier (Fig. 1) and Compound Sziklai amplifier (Fig. 2) and 1mV for cascade stage proposed amplifier (Fig. 3) at 1KHz frequency is drawn as input for the amplification purpose.

III. RESULTS AND DISCUSSIONS

The amplifiers of Fig. 1 and Fig. 2 are found to provide undistorted output in 10-30mV range of AC input signal at 1KHz frequency while the proposed two-stage amplifier (Fig. 3) produces distortion-less results in 1-15mV range of AC input at similar frequency [10], [11].

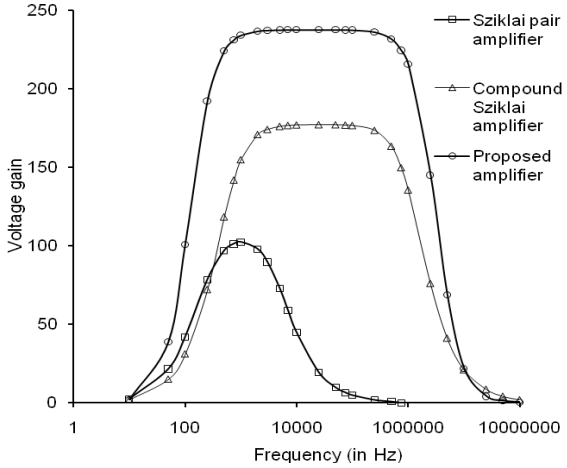

Fig. 4. Variation of voltage gain with frequency

Variations of maximum voltage gain as a function of frequency for all the three amplifiers are depicted in Fig. 4. It is found that the Sziklai pair amplifier (Fig. 1) produces 102.309 maximum voltage gain (1.106 volts peak output voltage), 7.345 maximum current gain (110.6 μA peak output current) with a narrow bandwidth of 4.80 KHz (lower cut-off frequency f_L=224.453Hz and upper cut-off frequency f_H=5.0556KHz) [10]. Similarly, the Compound Sziklai amplifier (Fig.2) crops an enhanced voltage gain of 177.006 (1.554 volt peak output voltage), reduced current gain of 5.059 (155.435μA peak output current) with wider 1.2091MHz bandwidth (f_L=547.54Hz and f_H=1.2097MHz) [11]. However, the proposed two-stage amplifier (Fig.3) produces considerably improved voltage gain of 237.505 (254.540 milli-volt peak output voltage) with multiplicatively enhanced current gain of 339.948 (25.454μA peak output current) and 2.003MHz bandwidth (f_L=183.864Hz and f_H=2.0458 MHz).

It is also to be mentioned that the output waveforms of Sziklai pair amplifier (Fig. 1) show 180 °phase shift with AC input signal while phase difference for Compound Sziklai amplifier (Fig. 2) is observed to be 228.6° [10]-[11]. However, for the proposed two-stage amplifier, this phase difference reduces to a considerable value of 151.2 °.

It is worth mentioning that if the circuits of Fig. 1 and Fig. 2 are simply cascaded to obtain two-stage Sziklai pair based amplifier, the output waveform bears severe distortion. However if emitter of transistor Q3 is connected to node-12 (i.e. with collector of transistor Q4 in Fig. 3) instead of V_{CC} at

node-4 (Fig. 3), the resultant voltage gain falls down below unity with undistorted output waveforms.

In this sequence, author also attempted to verify the performance of the proposed circuit with the inclusion of missing-biasing-resistance of Stage-2 amplifier (which was initially available in circuit of Fig. 2 as R_1) between node 4 and 8 (in the circuit of Fig. 3). The maximum voltage gain, current gain and bandwidth in this situation are found to be 217.00, 320.074 and 2.345MHz respectively with 234.417mV peak output voltage and 23.442μA peak output current. Hence, it is clear that if the circuit of Fig. 1 with modification and the circuit of Fig. 2 without modification are cascaded to obtain Sziklai pair based two-stage small-signal amplifier, respective gains and bandwidth reduce.

Similarly, if R_{11} is raised to 100KΩ instead of mentioned value in Table I, the maximum voltage gain of the proposed circuit (Fig. 3) climbs up to 260.792 but the output waveforms are partially clamped towards the negative side of the axis. On the other hand, if R_{11} and R_{12} both are simultaneously increased the resultant voltage gain shows an enhancing tendency with the presence of partial clamping effect.

Total Harmonic Distortion (THD) percentage is also calculated for the proposed two-stage amplifier (Fig. 3) for 7 significant harmonic terms using standard formula [1], [2], [10] and found to be 1.935%. This is greater than THD for Sziklai pair amplifier (1.72% for 8 significant harmonic terms) but lower than compound Sziklai amplifier (4.154% for 6 significant harmonic terms).

TABLE II: VARIATION OF MAXIMUM VOLTAGE GAIN (AVG) AND MAXIMUM CURRENT GAIN (AIG) WITH TEMPERATURE

Temp. ℃	Circuit of Fig.1		Circuit of Fig.2		Circuit of Fig.3	
	A_{VG}	A_{IG}	A_{VG}	A_{IG}	A_{VG}	A_{IG}
-30	83.43	5.74	152.22	3.88	220.76	267.58
-20	86.93	6.02	156.96	4.09	224.24	281.76
-10	90.36	6.31	161.52	4.29	227.47	295.32
0	93.70	6.59	165.93	4.50	230.47	308.24
10	96.96	6.87	170.16	4.70	233.24	320.52
27	102.31	7.34	177.00	5.05	237.50	339.94
50	109.12	7.96	185.54	5.52	242.40	363.09
80	117.22	8.73	195.50	6.12	247.48	389.34

Variation of maximum voltage and current gains with temperature is also measured for the amplifiers under consideration. Respective observations are listed in Table II. It is found that both voltage and current gain increase with rising temperature for all the three amplifiers. This observation verifies the usual behaviour of transistor parameter h_{FE} with temperature [13], [14]. It is worth mentioning that for proposed two-stage amplifier (Fig. 3), voltage gain and current gain both are higher than the other two amplifiers (of Fig. 1 and Fig. 2) at every temperature. Author also observed the variation of bandwidth with temperature and found that the bandwidth of all the amplifiers remain almost unaltered with temperature, hence the observations are not listed in Table II.

Variation of maximum voltage gain with added resistances for amplifiers of Fig. 1 and Fig. 2 is shown in Fig. 5. The maxim of voltage gain corresponding to R_D for Sziklai Pair amplifier is observed at 0.5KΩ [10]. The overall property is that the voltage gain linearly decreases up to R_D=50KΩ, thereafter, it tends towards saturation. Thus Sziklai Pair amplifier is found to produce considerable response at R_D=0.5KΩ, whereas for amplifier of Fig. 2, maximum voltage gain rises with increasing values of R_{D1} (at constant R_{D2}) from 0.5KΩ to 50KΩ, thereafter, tends towards saturation. However it increases with increasing values of R_{D2} (at constant R_{D1}) up to 150KΩ and beyond this critical limit it suddenly drops and tends towards saturation [11].

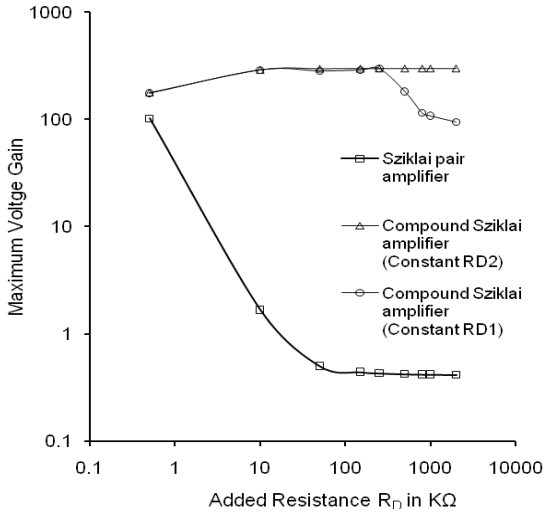

Fig. 5. Variation of maximum voltage gain with added biasing resistances

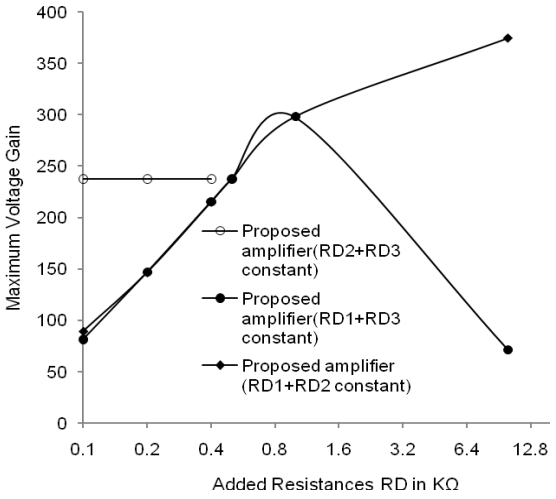

Fig. 6. Variation of maximum voltage gain with added biasing resistances for proposed amplifier

In addition, the variation of maximum voltage gain with added resistances for proposed two-stage amplifier (Fig. 3) is shown in Fig. 6. Maximum voltage gain remains almost unaltered at increasing values of R_{D1} up to 0.4KΩ (at constant R_{D2} and R_{D3}) beyond which the amplifier does not respond properly. On the other hand, it raises almost linearly with increasing values of R_{D2} up to 1KΩ (at constant R_{D1} and R_{D3}), thereafter, it decreases rapidly up to 10KΩ and beyond this critical limit amplifier seizes to work. However, maximum voltage gain gradually enhances with R_{D3} (at constant R_{D1} and R_{D2}) up to 10KΩ, thereafter, the amplifier does not respond with fair output.

Attempts are also made to assess the performance of proposed two-stage amplifier in absence of added resistances R_{D1}, R_{D2} and R_{D3}. When R_{D1} is removed from the proposed

circuit, resultant voltage gain of the amplifier increases to 243 with undistorted output waveforms but a problem stems in its frequency response. At higher frequencies its response becomes poor almost in the same way as is usually observed for conventional small-signal Darlington pair amplifier [3],[4]. However if either of the remaining added resistances R_{D2} or R_{D3} is removed from the proposed circuit the resultant voltage gain of the amplifier climbs down to a considerably low limit with unavoidable amount of distortion in the output waveforms.

Conclusively, high driving voltages received by the composite units of Stage-1 and Stage-2 circuits (10.631volts for Stage-1 and 17.178volts for Stage-2) and the combination of added resistances R_{D1}, R_{D2} and R_{D3} is responsible to maintain gain performance and to reduce harmonic distortion of the proposed two-stage amplifier.

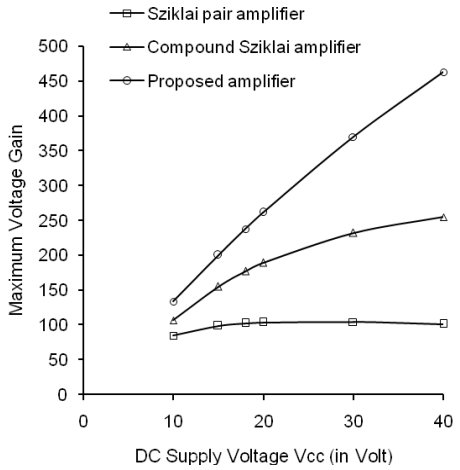

Fig. 7. Variation of maximum voltage gain with supply voltage

Variation of maximum voltage gain with V_{CC} is depicted in Fig. 7. For the amplifier of Fig. 1, it rises non-linearly at increasing values of V_{CC} up to 20V and beyond this critical limit it decreases with a slow pace [10] whereas the maximum voltage gain for amplifier of Fig. 2 increases almost exponentially with increasing values of biasing voltage up to 40V [11]. However, maximum voltage gain increases almost linearly at increasing values of DC biasing voltage V_{CC} for proposed two-stage amplifier (Fig. 3). The optimum performance of all the three amplifiers is received for 10-40V voltage range of V_{CC}.

Variations in maximum current gain with DC supply voltage V_{CC} are also observed but not shown graphically. At lowest permissible value of V_{CC} for optimum performance i.e. at 10V, the proposed amplifier provides a considerably high current gain of 216.90 whereas for amplifiers of Fig. 1 and Fig. 2 it is only 7.82 and 5.20 respectively. Similarly at the highest permissible value of V_{CC} i.e. at 40V, the proposed amplifier provides a considerably high current gain of 460.43 whereas for amplifiers of Fig. 1 and Fig. 2 it is merely 6.66 and 4.81 respectively. It is observed that the maximum current gain falls gradually with increasing value of supply voltage V_{CC} for Fig. 1 and Fig. 2 amplifiers while it shows a nonlinear gradual enhancement with increasing value of V_{CC} for amplifier of Fig. 3.

Variation of maximum voltage gain as a function of R_E for all the three amplifiers is traced in Fig.8. The voltage gain for amplifier of Fig. 1 increases almost exponentially with R_E [10] whereas it remains almost unaltered for other two amplifiers corresponding to any change in R_E. All the three circuits show an optimum performance in 0.5KΩ- 25KΩ range of R_E and above this value, the output waveforms show distortion.

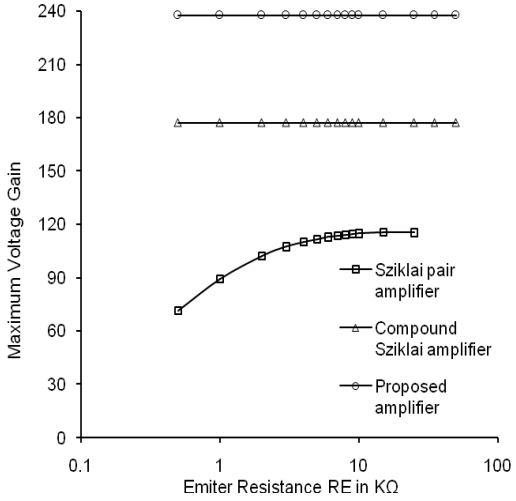

Fig. 8. Variation of maximum voltage gain with emitter resistance

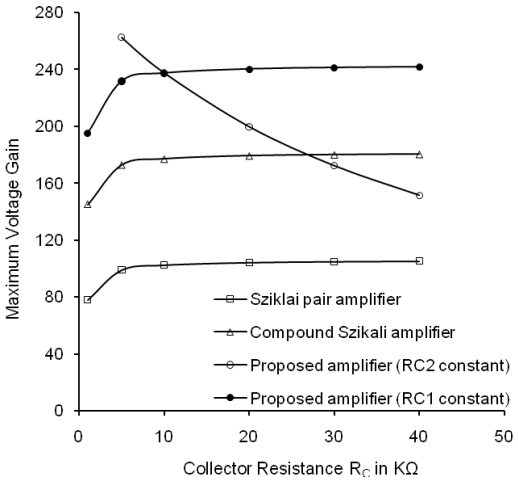

Fig. 9. Variation of maximum voltage gain with collector resistance

Variations of maximum voltage gain with collector resistance R_C / R_{C1} / R_{C2} is also estimated and shown in Fig. 9. It is found that maximum voltage gain has a nonlinear rising tendency for increasing values of collector resistance R_C for amplifiers of Fig. 1 and Fig. 2 up to 10KΩ and beyond this critical limit it gradually acquires a saturation tendency [10]-[11]. The similar situation prevails for proposed amplifier when R_{C1} is kept constant and R_{C2} is varied. But when situation is reversed, i.e. when R_{C2} is kept constant and R_{C1} is varied, the voltage gain of proposed amplifier decreases almost exponentially. It is also observed that voltage gain of the proposed amplifier is always higher than other two amplifiers at every value of collector resistance.

Variation of maximum voltage gain with R_L is also observed (graph not shown) for all the amplifiers and found well in accordance with the usual behaviour of small signal amplifiers [13]. Usual behaviour is also seen for current gain with varying load resistance R_L i.e. at lower values of R_L, current gain is high and vice-versa [13]. It is also worth mentioning that current gain of proposed amplifier corresponding to different values of R_L is found to be approximately equal to the product of the current gain of individual stages [13].

IV. Conclusion

Sziklai pair topology is normally used to design quasi-complimentary-symmetry push-pull Class-B power amplifiers but in the present manuscript it is explored to design a two-stage small-signal amplifier.

Proposed two-stage amplifier simultaneously produces high voltage and current gain with wider bandwidth than other two Sziklai pair based amplifiers. High driving voltages to Stage-1 and Stage-2 composite units as well as added resistances R_{D1}, R_{D2} and R_{D3} seem responsible for multiplicatively high current gain and considerably enhanced voltage gain and to reduce harmonic distortion of the proposed two-stage amplifier. The proposed amplifier will be useful for those applications where high voltage and current gain is the prime requirement of amplification in a wider frequency range which is approximately spanned from 200Hz to 2.5MHz. The proposed circuit successfully removes the poor response problem of conventional Darlington pair amplifiers at higher frequencies and narrow bandwidth problem of small-signal Sziklai pair amplifier.

The proposed amplifier shows a considerable response for additional biasing resistances R_{D1} up to 400Ω and for R_{D2} and R_{D3} up to 10KΩ. The optimum performance of the proposed amplifier is received for 10-40 volts of DC supply voltage and the maximum voltage gain remains unaffected for any change in emitter resistance R_{E1} or R_{E2}.

First two amplifiers provide distortion-less performance in 10-30mV range of AC input at 1KHz whereas this range for proposed amplifier is 1-15mV.

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