Turbo Decoder Design Employing a New Phase Estimation Hard Decision Stopping Criterion Method

Wen-Ta Lee and Yao-Chang Chang

***Abstract*—In this paper, a VLSI architecture of turbo decoder employing an efficient stopping criterionis proposed. The new stopping criterion algorithm is based on Hard Decision Aided(HDA) stopping criterion algorithm, using phase estimation method to reduce iterations also improve turbo decoding efficiency. In high SNR environment, the proposed algorithm requires less iterations without losing error correction ability compared to traditional stop criteria algorithms. In addition, it can save power consumption due to decoding termination within single iteration. As for low SNR environment, we can stop iteration immediately when it detect the received data can not be decoded. The proposed algorithm can stop the turbo decoder earlierthan traditional methodsin both high SNR and low SNR environment. Finally, for verifying the proposed algorithm, a turbo decoder using new phase estimation is designed with TSMC 0.18µm 1P6M process, the chip size is 1530µm × 1504µm and working frequency is 48MHz.**

***Index Terms*—Turbo decoder, stopping criterion, phase estimation, hard decision.**

I. Introduction

Turbo coding has an excellent error correction capability by utilizing an iterative algorithm, which allows its coding gain near to Shannon-limit [1]. Nowadays, some of channel coding standards, such as 3GPP/3GPP2, IEEE802.16d/802.16e, global system mobile (GSM), and code division multiple access (CDMA) have chosen it as their optional channel decoder.

Turbo decoder is consisted of two necessary Soft-In Soft-Out (SISO) decoders. These two SISO decoders perform an iterative algorithm and exchange information from one to the other. The operation acts among two SISO decoders named iteration, which decides themajor decoding latency and power consumption of turbo decoder. Here, the procedure combines with sequential and interleaved phase decoding called an iteration. Normally, a specified number of maximum iteration is set for terminating decoding. A considerableissue is not every iteration can increasingly improve the decoding performance. Therefore, some researches choose log likelihood ratio (LLR) or Extrinsic values[2] as their criteria to determine when to stop decoding. The well known two earlier stop iteration algorithms areSign Change Ratio (SCR) algorithm andHard Decision Aided (HDA) algorithm [3]. SCR algorithm needsto consider the threshold value very carefully because the chosen valueaffects the coding gain significantly. The criterion of HDA algorithm is to compare the hard decision bits between two iterations and to terminateiteration when the comparison remains the same result. A modification of HDA algorithm called HDA-DHDD algorithm [4] is proposed in 2005. It stops the iteration when DHDD satisfy the threshold value.

Generally speaking, many earlier stop iteration algorithms terminate their decoding after completing a single iteration. In this paper, a new stopping iteration algorithm based on phase criterion is proposed. Thus, it can give the ability to reduce decoding latency and save power consumption.

This paper is organized as follows. Section II introduces the turbo encoder and decoder. In Section III, we describe a new stop criterion algorithm based on phase estimation that can improve decoding efficiency. Section IV illustrates the architecture of proposed turbo decoder. Conclusionsare given in Section V.

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II. Turbo Encoder and Decoder

A. Turbo Encoder

The turbo encoder is composed of two parallel concatenated recursive systematic convolutional (RSC) encoders [5]. The first element encoder receives uncoded (systematic) data bits u_k in order and outputs a set of parity bitsx_1^p. The second element encoder receives a permutation of the uncoded data bits from a block interleaver and outputs a second set of parity bitsx_2^p. The systematic bits and the two set of parity bits are sent to the channel. It is shown in Fig. 1.

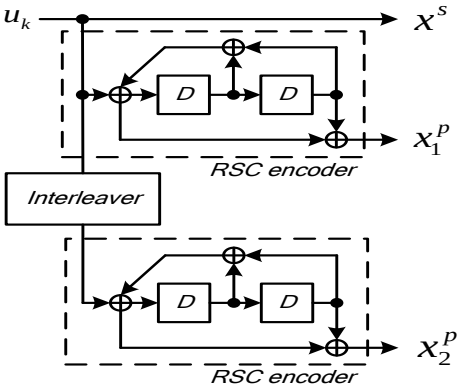

Fig. 1. Block diagram of turbo encoder.

B. Turbo Decoder

The turbo decoder is made up of two elementary SISO decoders. Each SISO decoder has three input ports: y_s is the received systematic bit from the channel, y_p is the received parity bit from the channel, and L_i is called priori LLR. Two output ports: L_e is the extrinsic information bit, L_r is the LLR. Theturbo decoder diagram is shown in Fig. 2[6]. In initial setting, the $L_{2-deint}^e$ set to zero. When SISO1 receives the

y_s and y_{p1}, it generates L_1^e and feeds it to the interleaver circuit, and then the interleaver circuit outputs L_{1-int}^e as the priori LLR of SISO2. When SISO2 receives interleavered value y_{s-int} , y_{p2} and L_{1-int}^e , it transports L_1^e to deinterleaver circuit, and then deinterleaver circuit sends $L_{2-deint}^e$ to SISO1. Repeat above procedures until turbo decoder produces a reliable soft out. A completed iteration is defined as theoperation among two SISO decoders exchanges their information iteratively. The soft out data, $L_2(\hat{u})$ is deinterleavered by deinterleaver circuit and input to the hard decision block to extract sign bit[7].

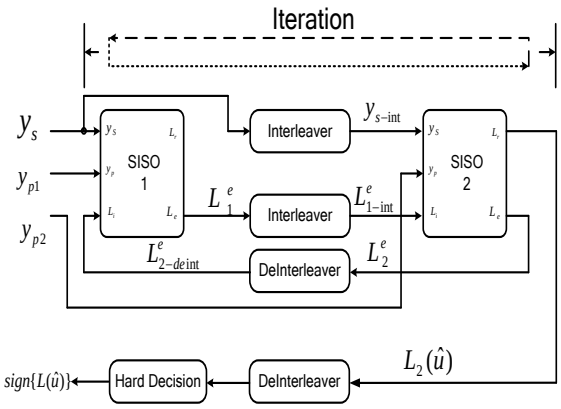

Fig. 2. Diagram of traditional turbo decoder.

III. Phase Estimation Hard Decision Stop Criterion

A. Concept of Proposed Stop Criterion

Traditional stop criteria use iteration as computing cycle to check its stop condition [8-11]. In this section, a phase estimation stopping criterion based on HDA algorithm is proposed. The proposed algorithm is called Phase Estimation Hard Decision (PEHD) stopping criterion. It operates the stop criterion after one phase operation is completed. We call the operation of decoding in SISO1 as sequential phase and in SISO2 as interleaverd phase, the diagram is shown in Fig. 3. PEHD algorithm not only reduces total numbers of iteration in high SNR, but also can detect the damaged degree of received data and terminate immediately in low SNR.

First, PEHD algorithm compares $L_1(\hat{u})$ with $L_2(\hat{u})$ when every phase operation completed in stop criterion operation circuit as Fig. 3 shows. When sign{L($\hat{u}$)} is exact, that implies $L_1(\hat{u})$ and $L_2(\hat{u})$ are constant values even doing further iteration decoding. In other words, $L_1(\hat{u})$ could be exact values before $L_2(\hat{u})$ when turbo decoding is successful.

As Fig. 3 depicts, $L_1(\hat{u})$ is generated in sequential phase but $L_2(\hat{u})$ is generated in interleaverd phase. Therefore, it has to confirm that the data order of $L_1(\hat{u})$ and $L_2(\hat{u})$ must be the same before to do stop criterion operation. When error is free, the relationship between $L_1(\hat{u})$ and $L_2(\hat{u})$ are listed below:

$$L_1(\hat{u}) = L_2(\pi^{-1}(\hat{u})) \quad (1)$$

$$L_2(\hat{u}) = L_1(\pi(\hat{u})) \quad (2)$$

where π is aninterleaverfunction, π^{-1} is a de-interleaverfunction.

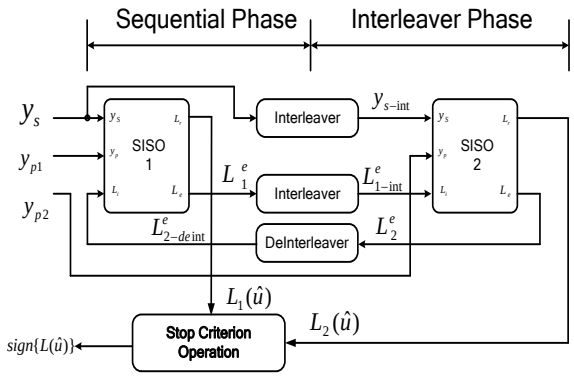

Fig. 3. Structure diagram of proposed turbo decoder.

In terms of above descriptions, when $L_1(\hat{u})$ is compared with $L_2(\hat{u})$ in sequential phase, $L_2(\hat{u})$ has to be deinterleavered to confirm their data order are the same first. Similarly, $L_1(\hat{u})$ has to be interleavered before $L_2(\hat{u})$ compared with it in interleaverd phase.

B. Decoding Convergence in High SNR

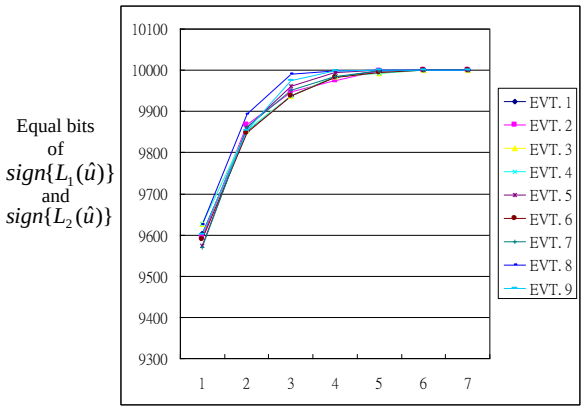

Fig. 4. Relationship diagram of sign{$L_1(\hat{u})$}, sign{$L_2(\hat{u})$}and number of phase operation in SNR 3Db.

Turbo decoder usually can correct all errors of received data successfully when it is in high SNR. In this situation, the relationship between sign{$L_1(\hat{u})$}, sign{$L_2(\hat{u})$} and phase operation times is shown in Fig. 4. Where sign{$L_1(\hat{u})$} and sign{$L_2(\hat{u})$} mean sign bits of $L_1(\hat{u})$ and $L_2(\hat{u})$. The simulation frame size is 10000 and SNR is 3dB. EVT1 to EVT9 are evaluation times 1 to 9.

Equal bits of sign{$L_1(\hat{u})$} and sign{$L_2(\hat{u})$} are getting higher and higher when times of phase operation are increasing.

Therefore, the equal bits between sign{$L_1(\hat{u})$} and sign{$L_2(\hat{u})$} are proportional to operation times of phase when turbo decoder in high SNR situation.

C. Decoding Divergence in Low SNR

On the contrast, turbo decoder can't correct all errors of received data successfully when it in low SNR. The relationship between sign{$L_1(\hat{u})$},sign{$L_2(\hat{u})$}and number of phase operation in low SNR is shown in Fig. 5. Where its frame size 10000 and SNR is 0 dB.

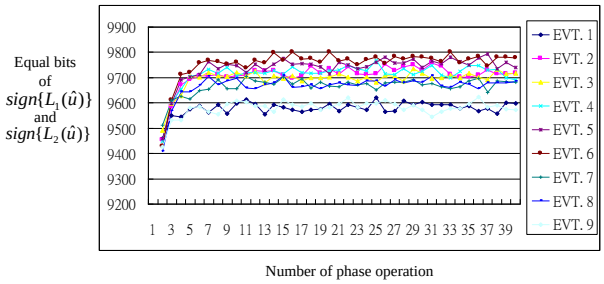

Fig. 5. Relationship diagram of sign{$L_1(\hat{u})$}, sign{$L_2(\hat{u})$}and number of phase operation in SNR 0dB.

Fig.5demonstrates equal bits relationship between sign{$L_1(\hat{u})$} and sign{$L_2(\hat{u})$} are random even operation times of phase are increasing.In other words, the relationship between sign{$L_1(\hat{u})$}and sign{$L_2(\hat{u})$}is irregular when turbo decoderis in low SNR situation.

D. New Stop Criterion

In order to satisfy decoding convergence and divergence conditions, the stopping criteria of proposed new algorithm are described as below:

1) If $sign\{L_1(\hat{u})\}$ of ith phase operation equals to $sign\{L_2(\hat{u})\}$ of (i-1)th phase operation totally in sequential phase, or$sign\{L_2(\hat{u})\}$of ith phase operation equals to $sign\{L_1(\hat{u})\}$ of (i-1)th phase operation totally in interleaverd phase, then the proposed algorithm stops turbo decoder.
2) If the equivalent values between $sign\{L_1(\hat{u})\}$ and $sign\{L_2(\hat{u})\}$ of ith phase operation are larger than (i+1)th phase operation, then proposed algorithm stopsturbo decoder.

In high SNR situation, turbo decoder usually can correct errors successfully and stop criteria conditions of four algorithms could be satisfied. Due to traditional stop criteria compute their stop criterion condition after one iterative decoding is completed, so they need at least two iterations to verify their stop criterion. It increases the decoding time and power consumption of turbo decoder.

The PEHD algorithm computes its stop criterion after every one phase operation completed as illustrated in Fig.6. That means it can compute its stop criterion twice in one iteration. Therefore, it only needs one iterative operation in best condition.

IV. Architecture of PEHD Turbo Decoder

The proposed algorithm is compared with other three stop criteria, HDA, SCR, and HDA-DHDD. The error correction performance of stop criteria is simulated on same turbo decoder platform and it is shown in Fig. 7.

Based on Fig. 7, it indicates the BER performance of PEHD algorithm is almost the same as other three stopping criteria.VLSI architecture of turbo decoder adopting PEHD algorithm is shown in Fig. 8, it is composed of SISO, received data buffers, interleaver and deinterleaver data ROM, extrinsic data buffers and PEHD stopping criterion circuit. PEHD algorithm needs a memory thatit can be read first and written last on same clock edge to store previous sign{$L_1(\hat{u})$}or sign{$L_2(\hat{u})$}.

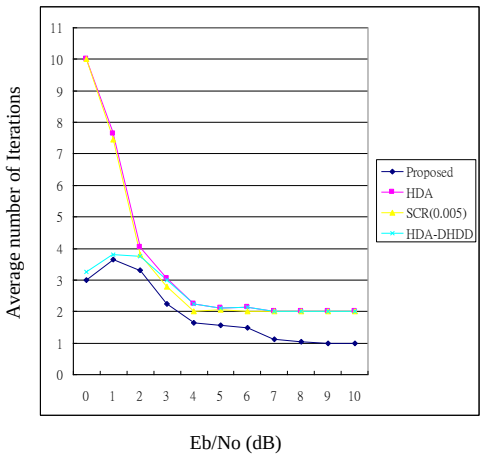

Fig. 6. Average numbers of iteration diagram of HDA, SCR, HDA-DHDD and proposed algorithm.

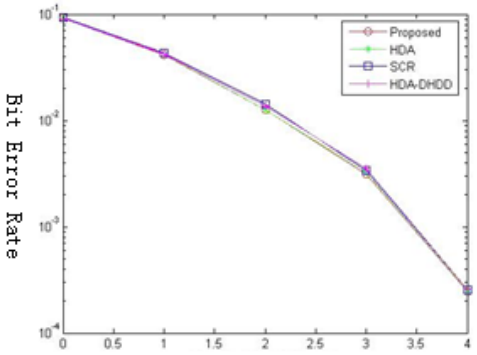

Fig. 7. BER performance of HDA, SCR, HDA-DHDD and proposed algorithm

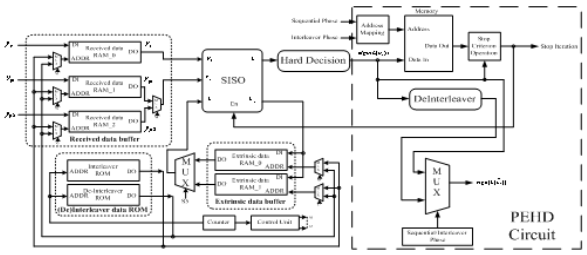

Fig. 8. Turbo decoder architecture with proposed algorithm

These stopping criteria are summarized in Table I. The PEHD algorithm has the earlier stop iteration function in both high SNR and low SNR environment. Moreover, it has less number of iterations and the total decoding timethat can save more power consumption compared to other algorithms.

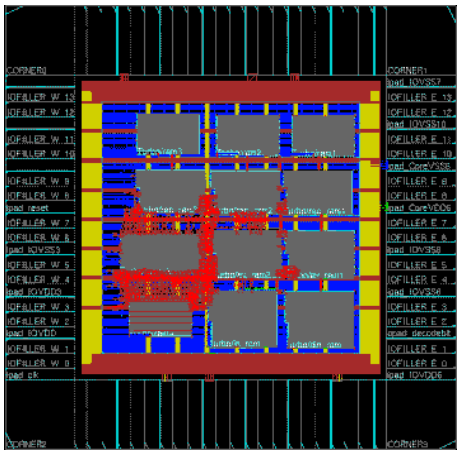

Fig. 9. Chip layout diagram with proposed stop criterion algorithm

TABLE I: COMPARISON TABLE OF STOPPING CRITERIA

Items / ***Algorithm***	***Stop Criterion***	***Minimum Iteration***	***Operation unit of stop criterion***	***Stop Criterion Demand***	
				High SNR	***Low SNR***
HDA	$\Delta sign\{L_2(\hat{u})\} = 0$	2	Iteration	Yes	No
HDA-DHDD	DHDD < (0.01)N	2	Iteration	Yes	Yes
SCR	C(i) ≦ (0.005)N	2	Iteration	Yes	No
Proposed	(a) When $sign\{L_{1(2)}(\hat{u})\}_i$ equals $sign\{L_{2(1)}(\hat{u})\}_{i+1}$ totally. (b) When ith equivalent value is larger than (i+1)th, between $sign\{L_1(\hat{u})\}$ and $sign\{L_2(\hat{u})\}$.	1	Phase	Yes	Yes

Finally, this new phase estimation hard decision stop criterion turbo decoder has been designed with TSMC 0.18μm 1P6M process. Table II shows the specifications of chip. The decoder chip size is 1530μm × 1504μm, working frequency is 48MHz. The chip layout is shown as Fig. 9.

TABLE II: SPECIFICATIONS OF PROPOSED TURBO DECODER

Process	TSMC 0.18μm 1P6M
Interleaver type	S-Random
Interleaver size	1024-bit
Constraint length	3
Generator Polynomial	(7, 5)
Code rate	1/3
Decoding algorithm	SW-Log-MAP
Sliding window size	16-bit
Total cells	18786
Operation frequency	48MHz
Chip area (include PAD)	1530μm x 1504μm

V. CONCLUSIONS

A new Phase Estimation Hard Decision stopping iteration criterion is proposed.It can stop the turbo decoder earlierthan traditional methodsin both high SNR and low SNR environment. In best condition, it only needs one iteration for turbo decoding. Thus, the proposed PEHD method can give a low-power and low-latencysolution for chip integration.

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