Analysis and Simulation of Subthreshold Leakage Current Reduction in IP3 SRAM Bit-Cell at 45 nm CMOS Technology for Multimedia Applications

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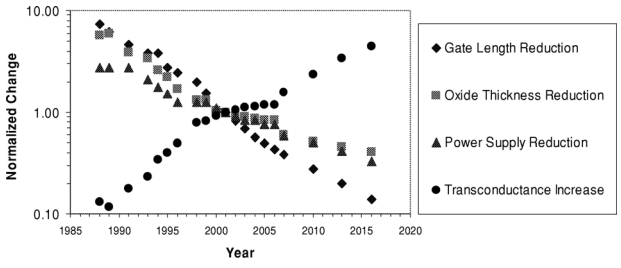
***Abstract*—Leakage currents in deep sub-micrometer regimes is becoming a significant contributor to power dissipation in CMOS digital circuits as the threshold voltage, channel length, and gate oxide thickness are reduced. Therefore, the identification and modeling of different leakage components is very important for the estimation and reduction of leakage power consumption, especially for battery powered and portable low-power applications. In this work we have performed an analysis and circuit level simulation at Deep Sub-Micron (DSM) Complementary Metal Oxide Semiconductor (CMOS) technology, pdk45nm. The simulation has been performed on the existing Static Random Access Memory (SRAM) cell structures, e.g., the conventional 6T, PP, P4, P3, and IP3 cells, to calculate the Subthreshold and standby leakage powers at V_{DD}=0.7V and 0.8 V. It is found that the IP3 Cell has minimum subthreshold leakage current (at standby mode), i.e., 90%, 95%, 50%, and 51% as compared to the 6T, PP, P4, and P3 cells, respectively at no performance and stability loss with a small area penalty. The standby leakage power is better in P4, and P3 cells by 59%, and 23% to IP3 cell but at the cost of degraded cells' data retentation and stability. The standby leakage power in IP3 is reduced by 36% and 52% in comparison with 6T and PP cell with improved cell stability and performance. The simulation has been carried out on t_{ox}= 2.4nm, V_{thn}= 0.22 V, V_{thp}= 0.224 V, V_{DD}=0.8 V, 0.7 V, T= 27 °C.**

***Index Terms*—SRAM, CMOS, low-power, gate leakage, leakage power, subthreshold current, oxide tunnelling.**

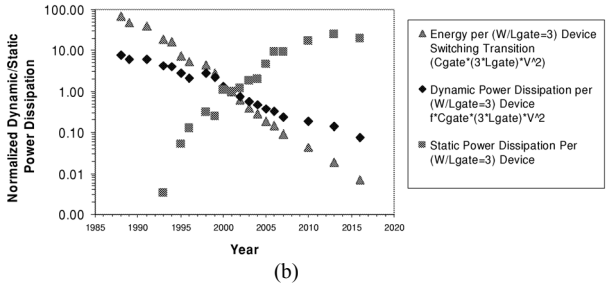
I. Introduction

To achieve high density, performance, and lower power consumption, CMOS devices have been continuously scaled for more than last 40 years. Transistor delay times decrease by more than 30% per technology generation, resulting in doubling of microprocessor performance every two years. The supply voltage (V_{DD}) has been scaled down in order to keep the power consumption under control. Hence, the transistor threshold voltage (V_{th}) has to be commensurately scaled to maintain a high drive current and achieve performance improvement. However, the threshold voltage scaling results in the substantial increase of the subthreshold leakage current [1-2].

Fig. 1, shows projections for transistor physical dimensions, supply voltage, and device power consumption according to the International Technology Roadmap for Semiconductors (ITRS) [3]. All the parameters are normalized to their values in the year 2001. In the scaled CMOS devices, the substantial increase in leakage current, the static power consumption is expected to exceed the switching power component in the overall power consumption unless effective measures are taken into consideration to reduce the leakage power, Fig. 1 (b). Even if supported by the lithography, the channel length of the devices can't be scaled down arbitrarily as it may affect the device performance because of its Short Channel Effects (SCEs).



(a)



(b)

Fig. 1. ITRS projections for transistor scaling trends and power consumption: (a) physical dimensions and supply voltage and (b) device power consumption [3].

In digital CMOS applications, the most undesirable SCE is the reduced gate threshold voltage at which the device turns ON, especially at high drain voltages. Hence, to take the best advantages of the new high-resolution lithographic techniques, new device designs, structures, and technologies need to be developed to keep SCEs under control at very small device geometries. In addition to gate oxide thickness and junction scaling, another technique to improve short-channel characteristics is well engineering. By

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changing the doping profile in the channel region, the distribution of the electric field and potential contours can be changed. The goal is to optimize the channel profile to minimize the off-state leakage while maximizing the linear and saturated drive currents. Super steep retrograde wells and halo implants have been used as a means to scale the channel length and increase the transistor drive current without causing an increase in the off-state leakage current [4]–[7], e.g., the subthreshold leakage, gate leakage, gate induced drain leakage currents, etc, as leakage current components. The other solutions that are becoming popular are the use of the high-k metal gate devices in order to reduced leakage power in DSM regimes.

This paper is organized as follows. In Section II, the functional view of a conventional 6T SRAM Bit-Cell is discussed in brief. Different leakage current components and subthreshold leakage current mechanism is considered in deep-sub-micrometer transistors in Section III. Section IV, present a brief view on the review on related work and simulation work is presented in Section V. Finally, the conclusion of the paper appears in Section VI.

II. SRAM BIT-CELL: A CONVENTIONAL APPROACH

The conventional SRAM (CV-SRAM) cell has six MOS transistors (‘4’ nMOS and ‘2’ pMOS), Fig.2. Unlike DRAM it doesn’t need to be refreshed as the bit is latched in. It can operate at lower supply voltages and has large noise immunity. However, the six transistors of an SRAM cell take more space than a DRAM cell made of one transistor and one capacitor thereby increasing the complexity of the cell [8].

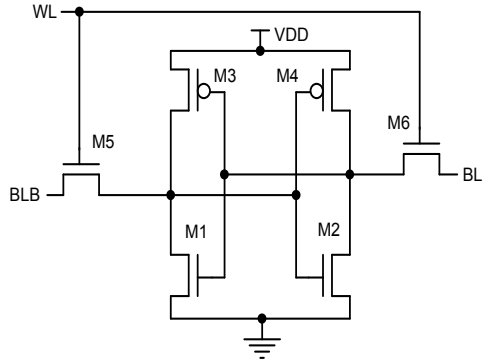

Fig. 2. 6T-CMOS SRAM Cell [8].

1) The SRAM Bit Cell

The memory bit-cell has two CMOS inverters connected back to back (M1, M3, and M2, M4). Two more pass transistors (M5 and M6) are the access transistors controlled by the Word Line (WL), Fig.2. The cell preserves its one of two possible states ‘0’ or ‘1’, as long as power is available to the bit-cell. Here, static power dissipation is very small. Thus the cell draws current from the power supply only during switching. But idle mode of the memory is becoming the main concern in the deep-sub-micron technology due to its concerns in the leakage power and data retentation at lower operating voltages.

2) The Operation of SRAM Bit-Cell

Although the two nMOS and pMOS transistors of SRAM memory bit-cell form a bi-stable latch, there are mainly the following three states of SRAM memory cell, the Write, Read, and Hold states.

A. Standby Operation (Hold)

When *WL*=‘0’, M5 and M6 disconnect the cell from Bit-Lines (BL and BLB). The two cross-coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are disconnected from the outside world. The current drawn in this state from the power supply is termed as standby current.

B. Data Read Operation

Read cycle starts with pre-charging BL and BLB to ‘1’, i.e., V_{DD}. Within the memory cell M1 and M4 are ON. Asserting the word line, turns ON the M5 and M6 and the values of *Q* and *Q*’ are transferred to bit-lines. No current flows through M6, thus M4 and M6 pull *BL* up to V_{DD}, i.e., *BL* = ‘1’ and *BLB* discharges through M1 and M5. This voltage difference is sensed and amplified to logic levels by sense amplifiers.

C. Data Write Operation

The value to be written is applied to the bit lines. Thus to write data ‘0’, we assert *BL*=0, *BLB* = ‘1’ and to write data ‘1’, the *BL* = ‘1’, *BLB* = ‘0’, asserted when WL = ‘1’.

III. LEAKAGE CURRENT MECHANISM IN DSM TECHNOLOGY

In DSM technology, the minimization of transistor off-state leakage current is an important issue for low-power circuit applications, especially in battery powered portable products. There are six short-channel leakage current mechanisms in DSM technology, Fig. 3. Here, I_1 is the reverse-bias pn junction leakage; I_2 is the subthreshold leakage; I_3 is the oxide tunneling current; I_4 is the gate current (due to hot-carrier injection); I_5 is the Gate Induced Drain Leakage (GIDL); and I_6 is the channel punchthrough current. The currents I_2, I_5, and I_6 are off-state leakage currents, while I_1 and I_3 occur in ON and OFF states, both. I_4 can occur in the off state, but more typically occurs during the transistor bias states in transition region.

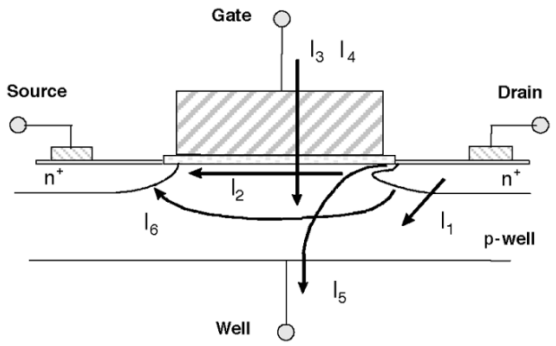

Fig. 3. A Summary of leakage currents in DSM CMOS transistors.

1) Reverse-Bias pn Junction Current (I_1)

In a MOS transistor, drain and source to well junctions are typically reverse biased, causes a reverse pn junction leakage current. A reverse-bias pn junction leakage (I_1) has two main components: one is minority carrier diffusion/drift (near the edge of the depletion region); and the other is due to

electron-hole pair generation (in the depletion region of the reverse-biased junction) [9]. For a MOS transistor, additional leakage can occur between the drain and well junction from gated diode device action (overlap of the gate to the drain-well pn junctions) or carrier generation in drain to well depletion regions with influence of the gate on these current components [10]. If both n and p regions are heavily doped (this is the case for advanced MOSFETs using heavily doped shallow junctions and halo doping for better SCE), band-to-band tunneling (BTBT) dominates the pn junction leakage [11].

2) Sub-threshold Leakage (I_2)

Sub-threshold (or weak inversion) conduction current between source and drain in a MOS transistor occurs when gate voltage is below V_{th} [12]. In the weak inversion, the minority carrier concentration is small, but not zero. Weak inversion typically dominates modern device off-state leakage current due to the low V_{th}.

The weak inversion current can be expressed as [12]:

$$I_{DS} = \mu_0 C_{ox} (W/L)(m-1) (V_T)^2 e^{(Vg-Vth)/mVT}(1-e^{-VDS/Vt}) \quad (1)$$

where,

$$m = 1+ C_{dm}/C_{ox}=1+ (\varepsilon_{si}/W_{dm})/(\varepsilon_{ox}/t_{ox})=1+3t_{ox}/W_{dm} \quad (2)$$

where,

V_{th}	: threshold voltage
V_T=kT/q	: thermal voltage (V_T=0.026V at RT)
C_{ox}	: gate oxide capacitance
ε_{si}	: permittivity of Silicon
ε_{ox}	: permittivity of oxide
μ_0	: zero bias mobility
m	: subthreshold swing coefficient
W_{dm}	: the maximum depletion layer width,
t_{ox}	: gate oxide thickness
C_{dm}	: capacitance of the depletion layer

3) Gate Oxide Tunneling Current (I_3)

It is the tunneling into and through the gate oxide. The reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from substrate to gate and also from gate to substrate through the gate oxide, resulting in the gate oxide tunneling current [13].

4) iv. Gate Current (I_4)

In short channel devices, the gate current appears due to the injection of hot-carriers from the substrate to gate oxide. The high electric field near the Si–SiO_2 interface, causes the electrons or holes to gain sufficient energy from the electric field and cross the interface potential barrier and enter into the oxide layer. This effect is known as hot-carrier injection. The injection from Si to SiO_2 is more likely for electrons than holes, as electrons have a lower effective mass than that of holes, and the barrier height for holes (4.5 eV) is more than that for electrons (3.1eV) [14].

5) Gate-Induced Drain Leakage Current (I_5)

The Gate Induced Drain Leakage (GIDL) current is a large component of off-state leakage current which is caused by Band-to-Band Tunneling (BTBT) in the drain region underneath the gate. When there is a large gate-to-drain bias, there can be sufficient energy-band bending near the interface between silicon and the gate dielectric for valence-band electrons to tunnel into the conduction band. The GIDL imposes a constraint for gate-oxide thickness scaling because the voltage required causing this band-to-band tunneling leakage current decreases with decreasing gate oxide thickness, and GIDL can pose a lower limit for standby power in memory devices [15].

6) Punchthrough Current (I_6)

In short channel devices and due to the proximity of the drain and the source, the drain current of a MOS transistor increases when a parasitic current path exists between drain and source. This part of the drain current is poorly controlled by the gate contact since the current path is located deeper in the bulk, farther away from the gate. It adds to the subthreshold leakage current leading to increased power consumption. Hence, punchthrough should be avoided whenever possible.

IV. Related Work–A Review

In this section, we review some of the previously proposed SRAM cell structures.

In [16], a novel low-stress SRAM cell has been proposed, named as IP3 SRAM bit-cell, as an integrated cell. It has a separate write sub-cell and read sub-cell, where the write sub-cell has dual role of data write and data hold. The data read sub-cell is proposed as a pMOS gated ground scheme to further reduce the read power by lowering the gate and subthreshold leakage currents. The drowsy voltage is applied to the cell when the memory is in the standby mode. Further, it utilizes the full-supply body biasing scheme while the memory is in the standby mode, to further reduce the subthreshold leakage current to reduce the overall standby power. The proposed IP3 SRAM Cell has a significant write and read power reduction as compared to the conventional 6T and PP SRAM cells and overall improved Read stability and Write ability performances. This design has given the overall standby and active power consumption but the individual subthreshold leakage current has not been calculated to address the leakage current during idle mode of the cell.

In [17] and [18], a P4, and P3 SRAM bit-cell structure at 45nm technology has been proposed for semiconductor memories with high activity factor based applications in Deep-Sub-Micron (DSM) CMOS technology. It has been proposed for the reduction of the active and the standby leakage power through the gate and sub-threshold leakage reduction in the active and standby mode of the memory operation [18]. The stacking transistor pMOS (PM4), connected in series (in line), is kept OFF in standby mode and kept ON in active (Read/Write) mode. The pMOS transistors are used to lower the gate leakage current [19] while full-supply body-biasing scheme is used to reduce the sub-threshold leakage currents. P3 SRAM bit-cell made a significant fall in dynamic as well as standby powers in comparison to the conventional 6T SRAM bit cell, at the cost of small area penalty and issues with SNM.

In [19], a gate leakage current reduction technique based on the pMOS pass-transistor SRAM bit-cell structure as PP-SRAM cell has been proposed at 45 nm technology and

0.8 V supply voltage. In this cell, in order to decrease the gate leakage currents of the SRAM bit cell, nMOS pass transistors are replaced by pMOS pass transistors. The use of pMOS leads to performance degradation due to different mobility coefficients for the nMOS and pMOS transistors. To overcome this problem, the width of pMOS pass transistor is selected as 1.8 times of that of the nMOS for technology used in this work.

V. Design and Simulation

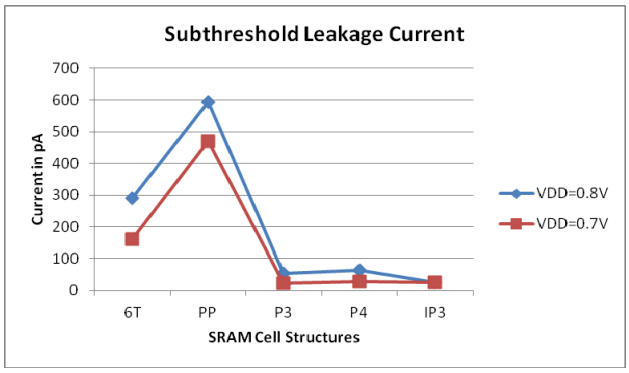

Fig. 4. Subthreshold leakage at V_{DD}=0.8 V and 0.7 V for 6T, PP, P4, P3, and IP3 Bit Cell

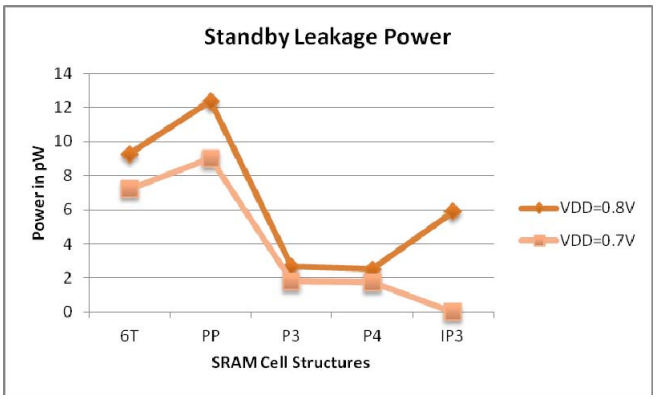

Fig. 5. Standby leakage power at V_{DD} =0.8 V, 0.7 V for 6T, PP, P4, P3, and IP3 Bit Cell

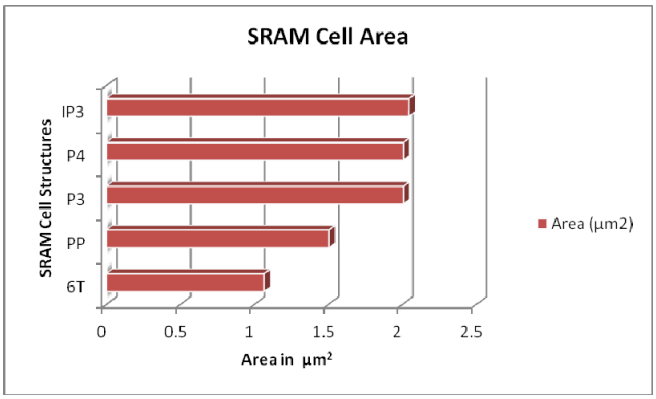

Fig. 6. Relative bit cell area of 6T, PP, P4, P3, and IP3

The simulation is being performed on the existing SRAM cell structures, the conventional 6T, PP, P4, P3, and IP3 cells as per the following simulation environment, at CMOS technology pdk 45 nm, supply voltage V_{DD}=0.8 V, and 0.7 V, gate oxide thickness t_{ox}=2.4 nm, threshold voltages, V_{thn}=0.22 V, V_{thp}=0.224 V, and operational temperature of T=27 °C (room temperature).

The Fig. 4, Fig. 5, and Fig. 6 shows the subthreshold leakage current, the standby power leakage, and the relative bit-cell's area, respectively, at the said simulation environment for the conventional 6T, PP, P4, P3, and IP3 SRAM cells.

VI. Conclusions

Leakage current is becoming a major contributor to the total power consumption in a System-on-Chip (SoC), as we are continuously scaling the CMOS devices. In current deep sub-micrometer devices with low threshold voltages, subthreshold and gate leakage have become dominant sources of leakage and are expected to increase with the technology scaling. To manage the increasing leakage in deep sub-micrometer CMOS circuits, solutions for leakage reduction have to be sought both at the process technology and circuit levels. At the process technology level, well-engineering techniques by retrograde and halo doping are used to reduce leakage and improve short-channel characteristics. At the circuit level, transistor stacking, multiple V_{th}, dynamic V_{th}, multiple V_{dd}, and dynamic V_{dd} techniques can effectively reduce the leakage current in high-performance logic and memory designs. We have performed an analysis and simulation on the Conventional 6T, PP, P4, P3, and IP3 SRAM Bit-Cells at V_{DD}=0.8 V and 0.7 V, t_{ox}=2.4 nm, V_{thn}=0.22 V, V_{thp}=0.224 V, and T=27 °C with all minimum sized and standard transistors. It is found that the IP3 Cell has minimum subthreshold leakage current (at standby mode), i.e., 90%, 95%, 50%, and 51% as compared to the 6T, PP, P4, and P3 cells, respectively at no performance and stability loss. The standby leakage power is better in P4, and P3 cells by 59%, and 23% to IP3 cell but at the cost of degraded cells' data retentation and stability. The standby leakage power in IP3 is reduced by 36% and 52% in comparison with 6T and PP cell with improved cell stability and performance. The performance-area trade-off penalty in IP3 cell is clearly visible which can be further optimized to reduce this trade-off in layout design.

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