A Novel Reversible Design of Unified Single Digit BCD Adder-Subtractor

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***Abstract*—Reversible quantum computer is the best choice for the future computer system. With the advent of quantum computer and reversible logic, design and implementation of all devices has received more attention. BCD digit adder is the basic unit of the more precise decimal computer arithmetic. Several proposals have been given for the BCD adders. This paper proposes a reversible implementation of 2:1 vector MUX and a combined BCD Adder / Subtractor. This paper can be extended to execute more complex operations using reversible logic.**

***Index Terms*—BCD adder-subtractor, decimal arithmetic, reversible logic, quantum computer, low-power VLSI**

I. Introduction

One of the major goals in VLSI circuit design is the reduction of power dissipation. R.Landauer demonstrated in the early 1960s, irreversible hardware computation results in energy dissipation due to the information loss, regardless of its realization technique [1]. It is proved that the loss of each one bit of information dissipates at least KTln2 joules of energy (heat), where K=1.3806505x10-23m2kg-2K-1 (joules Kelvin-1) is the Boltzmann's constant and T is the absolute temperature at which operation is performed [1]. Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information. Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2].

A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments [4-6].

Thus, the number of inputs and outputs in reversible logic circuits are equal. Such circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs [3]-[5].

Reversible logic has received significant attention in recent years. It has applications in various research areas such as Low Power CMOS design, quantum computing, nanotechnology and DNA computing. It is not possible to construct quantum circuits without reversible logic gates. Synthesis of reversible logic circuits is significantly more complicated than traditional irreversible logic circuits because in a reversible logic circuit, we are not allowed to use fan-out and feedback [4].

A reversible logic circuit should have the following features [5]:

- Use minimum number of reversible gates.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.

The output that is not used for further computations is called garbage output [9]. The input that is added to an n x k function to make it reversible is called constant input [9].

A reversible conventional BCD adder was proposed in [6] using conventional reversible gates – New Gates and Peres Gates. The implementation was improved in [7] using TSG reversible gates. An improved reversible implementation of decimal adder with reduced number of garbage is proposed in [8]. An optimized reversible BCD adder using new reversible gate (SCL Gate) was proposed in [9] which uses only 8 reversible gates, 6 constant inputs and produces only 8 garbage outputs. A reversible BCD Carry Look-Ahead Subtractor was proposed in [10]. The present work proposes a combined Reversible BCD Adder-Subtractor by using a reversible 9's Complementer circuit and a reversible 2:1 vector MUX.

The organization of this paper is as follows: Initially, necessary background on reversible logic gates those are used for the design is given. Then the proposed blocks are implemented using reversible gates. Then the proposed BCD Adder-Subtractor is implemented using reversible gates. Finally a comparative analysis of blocks has been given in terms of number of gates, constant inputs, number of garbage outputs and delay in terms of number of gates.

II. Reversible Logic Gates

This section describes the reversible gates those are used for the implementation of the proposed 2:1 vector MUX and BCD Adder / Subtractor.

Fig 1 shows a Feynman Gate [11]. Feynman Gate (FG) can be used as a copying gate. Since a fan-out greater that one is not allowed, this gate is useful for duplication of the required outputs. If the input vector $I_v = (A, 0)$, then the output vector becomes $O_v = (P = A, Q = A)$.

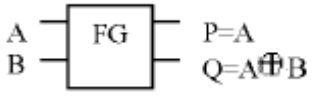

Fig. 1. 2 * 2 Feynman Gate (FG)

Fig 2 shows a Peres Gate (PG) [12]. It is also known as New Toffoli Gate (NTG). Functionally Peres Gate is equal

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with the transformation produced by a Toffoli Gate followed by a Feynman Gate.

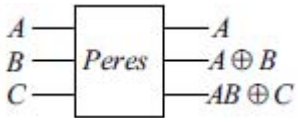

Fig. 2.3 * 3 Peres Gate (PG)

Fig 3 shows a HNG Gate (HNG) [13]. The reversible HNG gate can work singly as a reversible full adder. If the input vector I_V = (A, B, C_{in}, 0), then the output vector becomes O_V = (P=A, Q=C_{in}, R=Sum, S=C_{out}). It produces only two garbage outputs and requires only one constant input. It needs only one clock cycle to perform the operation. It is better in terms of hardware complexity.

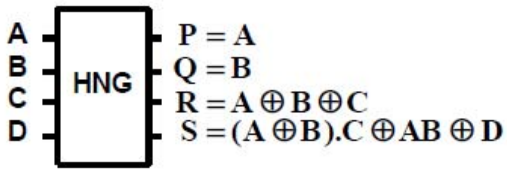

Fig. 3. 4 * 4 HNG Gate (HNG)

Fig 4 shows a TKS Gate (TKS) [14].

The TKS gate can be used to implement any Boolean function since two of its outputs (P & R) can function as 2:1 multiplexer.

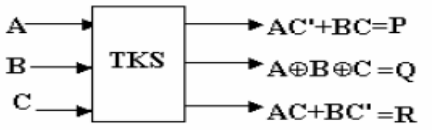

Fig. 4. 3 * 3 TKS Gate (TKS)

Fig 5 shows a SCL Gate (SCL) [9]. The SCL gate (Six Correction Logic) can be used for the correction in the BCD addition.

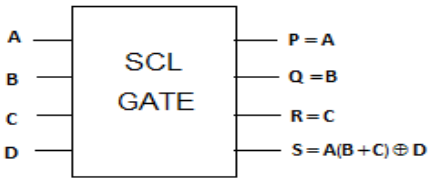

Fig. 5. 4 * 4 SCL Gate (SCL)

Fig 6 shows a BVF Gate (BVF) [15].

This is a reversible double XOR gate and can be used for the duplication of the required inputs to meet the fan-out requirements. This gate is used to copy the operand bits and the number of gates required to copy is reduced by 50% with same quantum cost. . If the input vector I_V = (A, 0, C, 0), then the output vector becomes O_V = (P=A, Q=A, R=C, S=C).

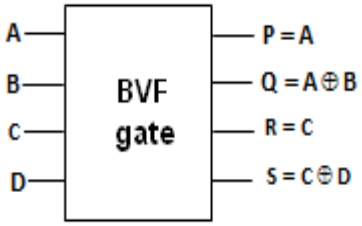

Fig. 6. 4 * 4 BVF Gate (BVF)

III. Nine's Complementer – Buffer

In the BCD subtraction, nine's complement of the subtrahend is added to the minuend. Instead of subtracting the number from nine, the Nine's complement of a number is computed by adding 1010 (equivalent to decimal 10) to the complement of the number. The nine's complementer circuit using a 4-bit adder and XOR gates is shown in Fig 7 [16]. The XOR gates are used as a Controlled NOT gate.

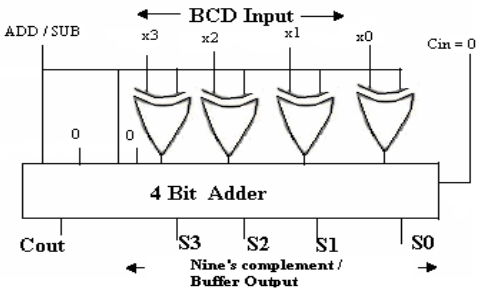

Fig. 7. Conventional nine's complementer – buffer

In the circuit, if ADD/SUB = 1, the input is complemented and added with 1010 to produce the nine's complement of the input. If ADD/SUB = 0 the circuit acts as a buffer. For the reversible implementation of the controlled NOT gate we have considered the complementer proposed in [10] which produces one garbage output. For reversible implementation of 4-bit parallel adder we have considered the circuit using HNG gates [17] since the hardware complexity is less. It has 4 constant inputs and produces 8 garbage outputs.

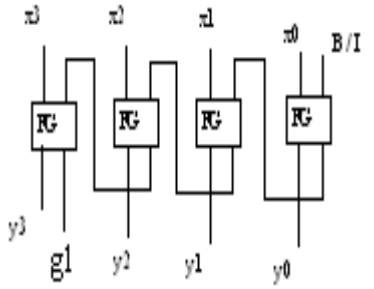

Fig. 8. Reversible controlled complementer-buffer

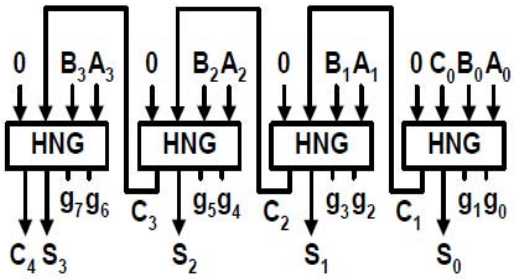

Fig. 9. Reversible 4-bit parallel adder

IV. Proposed Copying Circuit

Since fan-out of the outputs is not allowed in the reversible circuits, we propose a reversible circuit to copy 5-bit data. The proposed copying circuit is shown in Fig 10. It uses 2 BVF gates and one FG gate. It has 5 constant inputs and has no garbage output.

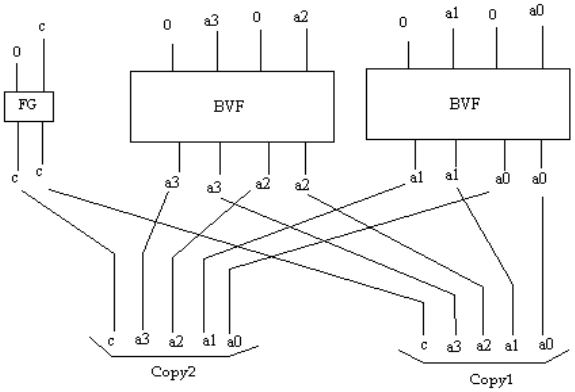

Fig. 10. Proposed Copying circuit

V. Proposed 2:1 Vector Mux

In TKS gate, using C input as a select pin, we can produce multiplexer output in the outputs P and R. In this proposed vector MUX, P output is considered as the primary output and R is considered as garbage output. This proposed vector MUX uses no constant input and produces 10 garbage outputs.

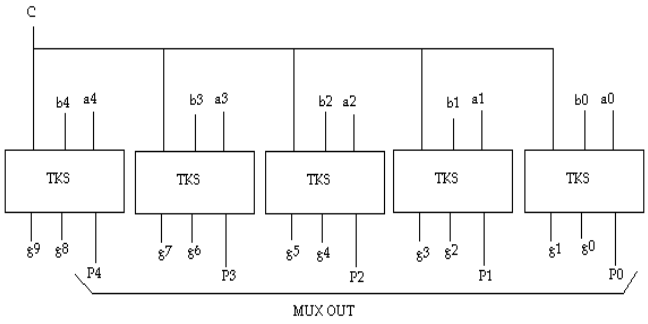

Fig. 11. 2:1 vector – MUX

VI. Proposed Bcd Adder-Subtractor

Fig 12 shows the circuit of the proposed single digit BCD Adder-Subtractor. This circuit is a modified version of the one proposed in [10]. Instead of the Carry Look-Ahead logic, parallel logic is used in this proposed method. This single circuit is capable of functioning as BCD Adder or BCD Subtractor depending on the ADD/SUB control input.

When the control input ADD/SUB = 1, the 9's complementer generates the nine's complement of the input digit B. This complemented data is added with the input digit A using 4-bit BCD adder [9] which uses 6 constant inputs and produces 10 garbage outputs. Two copies this output is generated using the copying circuit for the further process. One copy is given as the input to the complementer to produce the BCD subtracted output. This BCD Subtractor output is given as one of the input to the 2:1 5-bit vector MUX.

When the control input ADD/SUB = 0, the 9's complementer acts as a buffer. This buffered input is added with input digit A using 4-bit BCD adder. This output is copied and given as one of the input to the 2:1 5-bit vector MUX.

The proposed 2:1 5-bit vector MUX is used to produce the final output based on the control input ADD/SUB. When the control input ADD/SUB = 0, the BCD Adder output is routed to the output of the circuit. When the control input ADD/SUB = 1, the BCD Subtractor output is routed to the output of the circuit.

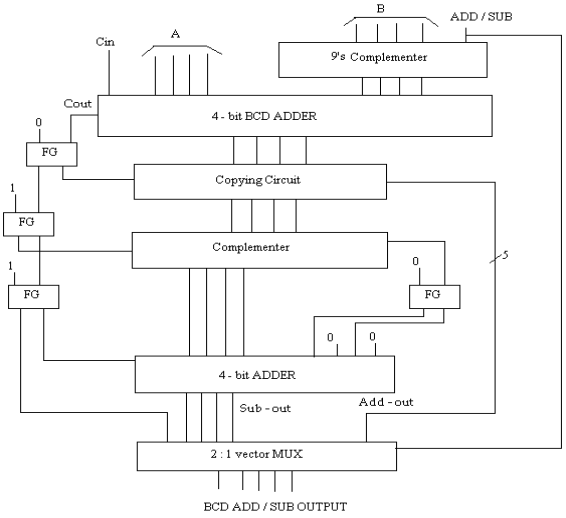

Fig. 12.Proposed BCD Adder-Subtractor circuit

VII. Results and Discussion

The proposed circuit uses a total number of 36 reversible gates consisting 14 Feynman gates, 13 HNG gates, one Peres gate, one SCL gate, two BVF gates and five TKS gates.

The total delay of the proposed design is calculated in terms of gate delays. The total delay $\tau_{total} = \tau_{9'sC} + \tau_{bcd\text{-}ad} + \tau_{copy} + \tau_{comp} + \tau_{4\text{-}bit\ ad} + \tau_{vect\text{-}mux} + 4FG$

where,

$\tau_{9'sC}$ = total delay in the 9's complementer-buffer circuit
= 4 FG + 4 HNG

$\tau_{bcd\text{-}ad}$ = total delay in 4-bit BCD Adder
= 1 FG + 5 HNG +1 PG + 1 SCL

τ_{copy} = total delay in copying circuit
= 1 FG + 2 BVF

τ_{comp} = 4 FG

$\tau_{4\text{-}bit\ ad}$ = total delay in the 4-bit adder = 4 HNG

$\tau_{vect\text{-}mux}$ = 5 TKS

Therefore τ_{total} = 36 gate delays

VIII. Conclusion

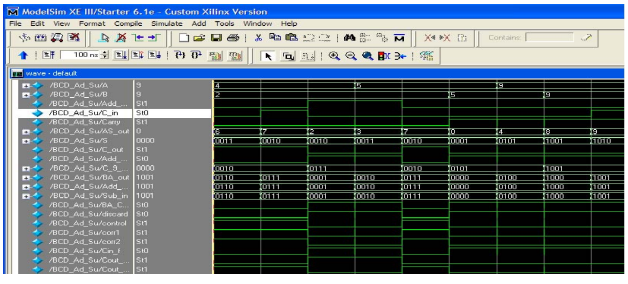

Fig. 13.Simulation results of BCD Adder-Subtractor

This paper proposes a unified BCD Adder-Subtractor circuit along with its reversible logic implementation. The logical verification was done using Xilinx ISE Simulator 9.1 and ModelSim 6.3C. The simulation result is shown in Fig 13. The proposed system can be used for designing large reversible systems. The analyses of various blocks discussed in the design are tabulated in Table-1.

TABLE I: ANALYSES OF VARIOUS BLOCKS

Parameters / Various Blocks	**No. of gates**	**No. of garbage outputs**	**No. of constant inputs**	**Delay in terms of no. of gates**
9's Complementer	8	9	4	8
4 – bit BCD Adder	8	10	6	8
Copying Circuit	3	0	5	3
Complementer	4	0	0	4
4 – bit Adder	4	8	4	4
2:1 vector MUX	5	10	0	5
Total design	36	37	25	36

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