0.69mW, 700MHz Novel 8x8 Digital Multiplier

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Abstract—**In this paper we presents the design of low power i.e 0.69mW and 700MHz, 8 x 8-bit digital multiplier providing a better performance and lower power dissipation than the conventional linear array multipliers in two folds of speed and power consumption. The modified pair-wise and parallel addition algorithms [2] provide high speed multiplication and lower power dissipation in this work. The power performance of individual block is pre evaluated to identify the most power consuming element and attempt is to select the most efficient topology to reduce the power consumption of entire multiplier while maintaining the high operating frequency. The proposed multiplier has been designed and implemented employing Tanner 0.18 μm CMOS technology and analyzed using TSPICE. When the multiplier is targeted to a maximum operating frequency of 700 MHz at VDD equal to 1.8 V, it dissipates 0.69 mW. For comparison purposes a Baugh-Wooley multiplier is redesigned and optimized. The simulation results are compared showing superiority of proposed multiplier in both power and speed performance.**

Index Terms—**Digital multiplier, low power, TSPICE, and 10-transistor full adder cell**

I. INTRODUCTION

Binary addition is one of the fundamental and essential arithmetic operations. It is frequently used to implement more complex functions such as multiplication, division, address calculation, and other many essential operations in microprocessors, DSPs and many different architectures. The next generation of wireless network requires high-speed and low power Digital Signal Processing (DSP) System-on-Chip (SoC). Amongst the building blocks of a DSP system a multiplier is an essential component that has a significant role in both speed and power performances of the entire system. Therefore to enhance the performance of DSP SoCs design of speed and power efficient multiplier is an asset. In this work we designed a multiplier by exploiting the high-speed capability of computational algorithm in a power-efficient architecture[1].

To achieve low-power performance for this architecture with its inherent high-speed characteristic low-power approaches encompassing the circuit design levels are investigated by identifying the most critical elements, selecting the suitable topology and designing the elements in

circuit level throughout an iterative approach to avoid over sizing or under sizing of transistors. This paper is organized as follows. Section 2 reviews the multiplication algorithm. The multiplier architecture and topology selection are described in Section 3. Section 4 presents the experimental results and comparison. The conclusion is drawn in Section 5.
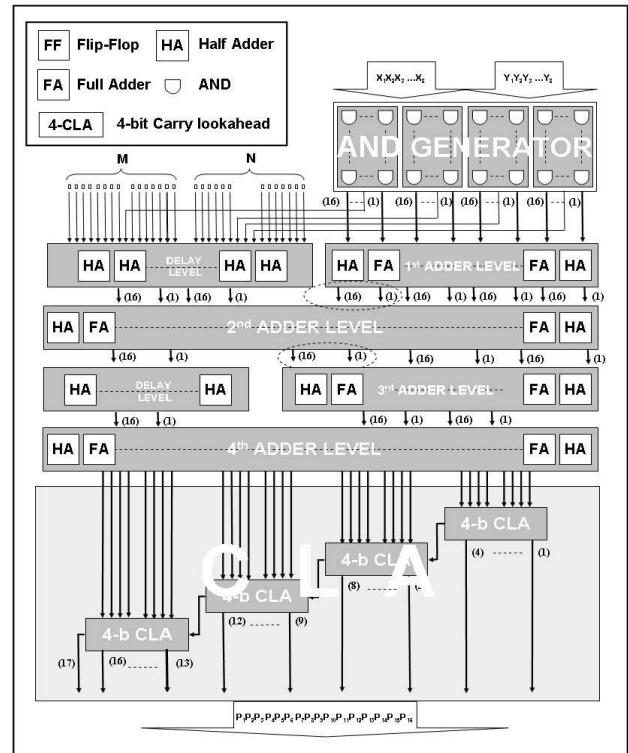

Fig. 1.Block diagram of the proposed multiplier

II. THE MULTIPLICATION ALGORITHM

A comparison of different multiplication algorithms [3] has revealed that for the operands equal to or greater than 16-b, tree architecture based on encoding techniques such as Booth algorithm and Wallace [4] provide higher performance with lower power dissipation than that of the array multiplier based on Baugh-Wooley or Braun algorithms [5]. For medium-bit operands (8-bit), however, the tree architecture multipliers are not power efficient and array architecture multipliers are not fast enough. Therefore, for an 8-bit multiplier a proper structure requires regularity of the array architecture and speed of tree architectures.

The pair-wise algorithm has capability of simplify the math in multiplying of two 8-b numbers without using any encoding technique. This algorithm carries out multiplication in two steps without using encoding technique. At the first step partial products are generated and then are added up in the second step to generate the final products. These two steps are briefly reviewed in this section, however a detail

explanation can be found in [2].

A. Partial Product Generation

Assume that x and y are two 8-bit numbers known as multiplicand and multiplier respectively.

$x=<x_8, x_7, x_6, x_5, x_4, x_3, x_2, x_1>$ $y=<y_8, y_7, y_6, y_5, y_4, y_3, y_2, y_1>$

x and y are then represented by sum of the two numbers (x_e, x_o and y_e, y_o) using even and odd positions of the multiplicand (x) and multiplier (y). Therefore,

$$x = x_e + x_o \quad y = y_e + y_o$$

where,

$x_e = <x_8, 0, x_6, 0, x_4, 0, x_2, 0>$, $x_o = <0, x_7, 0, x_5, 0, x_3, 0, x_1>$,
$y_e = <y_8, 0, y_6, 0, y_4, 0, y_2, 0>$, $y_o = <0, y_7, 0, y_5, 0, y_3, 0, y_1>$

In order to generate the partial products the even ($_e$) and odd ($_o$) terms of multiplicand and multiplier are multiplied pairwise. All the partial products $(P_{ee}, P_{eo}, P_{oe}, P_{oo})$ to generate the final product are explicitly shown in the following.

$$xy = (x_e + x_o)(y_e + y_o) = x_e y_e + x_e y_o + x_o y_e + x_o y_o$$

$$P = xy = P_{ee} + P_{eo} + P_{oe} + P_{oo}$$

The logic realization of $x_e y_e$ is shown in Fig. 2. This logic block can be used as a pattern for other partial products (P_{eo}, P_{oe}, P_{oo}). Note that the zero positions in the bit pattern alternate with the non-zero summations, which can be used to old the carry from the corresponding summation in the non-zero positions.

B. Partial Product Addition

The final multiplication product is the result of the addition of all partial products. Three-to-two adder technique is employed to reduce the number of the partial products. Using this technique three input bits are converted to two output bits. This can be simply done by a 1-b full adder. In the following the sequence of this operation generating two numbers at the final level of the multiplier is described (Fig. 3).

1. Each partial product $(P_{ee}, P_{eo}, P_{oe}, P_{oo})$ is represented by summation of two numbers corresponding to even and odd terms, namely, as follow (same method as used in partial product generation)
$$P_{ee} = P_{ee_e} + P_{ee_o}, \quad P_{eo} = P_{eo_e} + P_{eo_o}$$
$$P_{oe} = P_{oe_e} + P_{oe_o}, \quad P_{oo} = P_{oo_e} + P_{oo_o}$$

2. The even representatives of the first three partial products (P_{ee}, P_{eo}, P_{oe}) are added up so do the odd representatives. This addition is performed bit by bit via three-to-two technique, which results in converting three partial products (P_{ee}, P_{eo}, P_{oe}) to two numbers (A,B).

3. Four spars bits appearing in partial product equations generate two distinct numbers (M, N) (Fig. 1) as follow:

$M = <0, 0, 0, 0, 0, 0, x_7 y_1, x_2 y_7, x_2 y_8, 0, 0, 0, 0, 0, 0>$
$N = <0, 0, 0, 0, 0, 0, 0, x_7 y_2, 0, 0, 0, 0, 0, 0, 0>$

These two numbers together with P_{oo} are converted to another two numbers (C, D) in the same manner as the first three partial products (P_{ee}, P_{eo}, P_{oe}).

4. In this step four numbers (A, B, C, D) generated in step 2 and 3 need to be converted to two final numbers (G, H). This is done by repeating three-to-two conversion two more times Fig. 1.

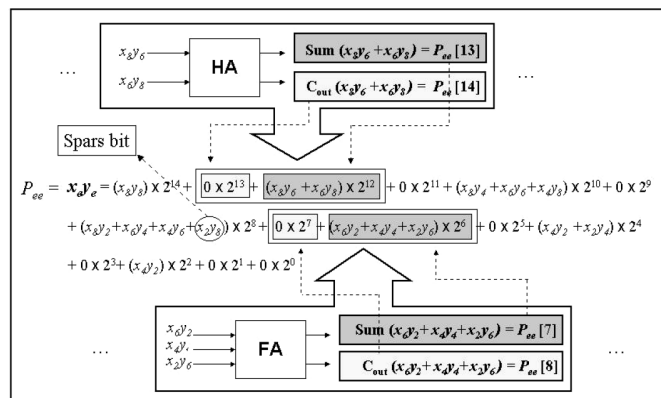5. Two 16-b numbers are added via CLA to generate the multiplication products.

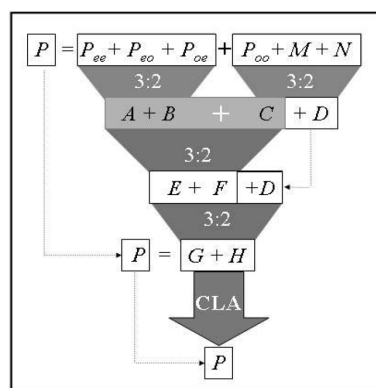Fig. 2. Partial product generation in pair-wise algorithm

Fig. 3. Partial product addition

III. MULTIPLIER ARCHITECTURE

Fig.1 shows the structure of the multiplier. An early analysis in proposed design results in identifying the block occupying a large portion of the total power and area. Here the adder levels consisting of full adder and half adder cells have significant impact on power and area of the entire design. Therefore, selecting an appropriate adder cell can significantly improve the performance of the multiplier.

Full Adder

Amongst many different adder cells introduced in literatures XOR and transmission gate [1], pseudo-NMOS, Transmission gate CMOS, complementary CMOS, complementary pass-transistors [5] and XOR and pass transistor logic are short-listed due to the low number of transistors. Based on the number of transistors, we decided to select an optimized design of the XOR and pass-transistor a new low-power adder[6]as shown in fig.4. This is an high performance Full adder cell has been designed using 10 transistors. The proposed cell has the advantage of low power consumption and high operating speed. Moreover, it occupies small area due to the small transistor count. This cell is achieved at the circuit level by reducing the number of internal node capacitances, by eliminating direct paths between the supply voltage and the ground, and by
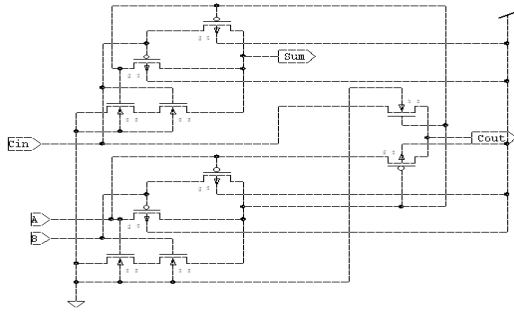
maintaining low switching activity in the circuit.

Fig. 4.10-Transistor Full adder cell

IV. EXPERIMENTAL RESULTS

Multiplier is simulated using XOR and pass transistor adder as standard cell as well as intermediate logic gates generating the final *Gi* and *Pi* signals of CLA block. Minimum operating frequency of the multiplier is determined based on worst case delay measurement described as follows.

Speed: is defined as the minimum interval (frequency) between two sequential multiplication operations (8-b x 8-b) for which the results of multiplication are successful. In the other word one can measures the worst case delay of the multiplier and simply calculate the minimum operating frequency of the multiplier using (2);

$$f_{min}=(\tau_{max})^{-1} \quad (2)$$

where f_{min} is the minimum operating frequency and τ_{max} is the worst case delay occurring in multiplication. More than 400 test patterns (350 random and 50 intentional) have been applied to the multiplier to verify the functionality and to measure the worst case delay. The worst delay has been observed when "FF" x "FF" (F= Hexadecimal representation of "1111").

TABLE 1: DELAY AND FREQUENCIES OF DIFFERENT CELLS

Circuit	Pre-Layout		Post-Layout	
	Delay (ps)	Frequency (GHz)	Delay (ps)	Frequency (GHz)
AND Gate	82.83	12.07	88.8	11.26
Half Adder	92.88	10.76	111.89	8.93
Full Adder	72.34	13.8	82.1	12.18
4-bit CLA	346	2.89	364.2	2.74
Multiplier (8x8)	1256	0.796	1420	0.704

This delay is recorded as 1256ps which is translated to 0.796 GHz minimum operating frequency. Fig 5 shows the composite format of simulation result. The delay and operating frequencies of the cells used in the multiplier pre and post layout simulation as shown in the Table1.

In order to evaluate the performance of our design, Baugh-Wooley multiplier is chosen, redesigned and optimized in the same manner as the proposed multiplier. Same adder cell is used in Baugh-Wooley multiplier as well as same structure for common logic gates. The average power

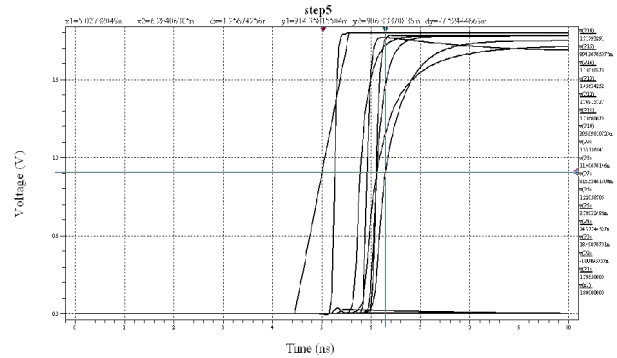dissipation of the cells used in multiplier is as shown in the Table 2.

Fig. 5.Simulation result of multiplication of "FF" x "FF"

TABLE 2: AVERAGE POWER DISSIPATION OF ALL CELLS

Circuit	Power Dissipation (µW)(Average Power)	
	Pre – Layout	Post - Layout
AND Gate	1.8	1.96
Half Adder	1.83	2.11
Full Adder	5.59	5.589
4 – bit CLA	45.7	48.03
Multiplier (8x8)	644	695

Speed and power of these two architectures are measured. The comparison result in Table 3 shows that the proposed multiplier not only consumes less power than that of its counterpart but also performs the complete multiplication of two 8-b numbers with much less delay. Table 4 shows the characteristics of the multiplier.

TABLE 3: CHARACTERISTICS OF THE PROPOSED AND BAUGH-WOOLEY MULTIPLIERS

Parameter	Proposed Multiplier	Baugh-Wooley Multiplier
Delay,ns	1.26	1.15
Power, mW	0.64	35.2

TABLE 4: PERFORMANCE OF THE PROPOSED MULTIPLIER

Device Characteristics	
Technology	6 Metal 180nm Digital CMOS
Supply Voltage (Vdd)	1.8V
Chip Characteristics	
Multiplier & Multiplicand	8 - bits
Product	16 - bits
Multiplication Delay	1256ps
Average Power Consumption	0.64 mW
Core Size	14.267mm^2

The proposed 8-b x 8-b multiplier is implemented employing 0.18µ CMOS technology. Layout of the complete multiplier is shown in Fig 6. Finally we are giving comparison of different multipliers in with proposed multiplier, designed by 10-Transistor full adder cell in Table 5.
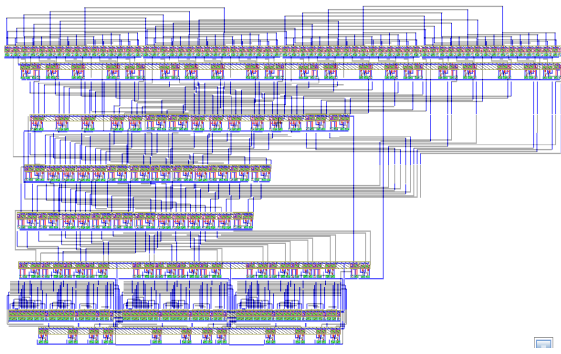
Fig. 6.The proposed 8-b x 8-b multiplier

V. CONCLUSION

This paper described a design of an efficient multiplier for 8-bit operands based on the multiplication technique using even and odd positions on multiplicand and multiplier to generate four n-bit numbers. The reasonable power consumption rate is also obtained by a conservative approach in topology selection. An early analysis on power performance of the multiplier identifies that adder levels have the major portion of power consumption. In order to select a power/speed efficient adder cell which is the building block of adder level six known adder cells are redesign and optimized. These adders are then compared for the final topology selection. Approximately 400 input patterns are applied to the multiplier to verify its functionality. TSPICE simulation results show that our multiplier can operate at 700 MHz in 0.18 μ CMOS technology under the supply voltage of 1.8 V. However, it is difficult to compare the performance of our design with others

TABLE 5.COMPARISION OF DIFFERENT MULTIPLIERS

Name of the Multiplier	Delay (µs)	Power (mW)
Baugh-Wooly Multiplier	2.8	83.5
Pipelined Multiplier	1.8	52.91
Novel Digital Multiplier	0.903	22.4
Proposed Multiplier(10-T)	1.256	0.64

directly due to different performance goals such as area against power or power versus speed, Baugh-Wooley architecture is redesign and optimized in a same method. Same structures are used for the logic gates and common elements for fair comparison. The experimental results show that our multiplier consumes 0.64mW of power consumption and performs the operation with less delay. Baugh-Wooley multiplier is not laid out therefore no comparison is made to assess the area of the multiplier; however its size is individually reported.

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