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Memory Reduced and Fast DDS Using FPGA

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***Abstract*—Direct digital synthesis is a method of creating arbitrary waveforms of desired frequency. A general DDS system comprises analog and digital part. Phase accumulator and LUT make digital part and DAC makes analog part. This paper presents 12 bit memory reduced FPGA based architecture of DDS. Phase truncation and quadrature symmetry of sine wave are used to achieve higher ROM compression. Dither is also used to achieve error free output. This design has been implemented on SPARTAN-3E FPGA with maximum clock frequency of 50 MHz. We have used LTC2624 quad DAC with 12 bit resolution which introduces very less amount of harmonics hence LPF is not needed. This design uses only 128 memory locations. Hence it is suitable for applications where system speed, memory and size of the system are main concern. Its wide and flexible range of frequency make it useful in RF transmission, Biomedical function generators and Modulation.**

***Index Terms*—Direct digital synthesis (DDS), Phase truncation, ROM compression**

I. Introduction

Dds is a technique to construct a waveform of desired frequency just by changing one input [1]. Now a days DDS is gaining preference because of its simple architecture. But small size and less power consumption is prime requirement. To reduce the memory and to increase system speed, we have employed phase truncation and quadrature symmetry and to reduce the errors generated by phase truncation a dither model of DDS is presented. To increase the efficiency and system speed, the whole architecture is implemented on SPARTAN 3E FPGA, and used onboard LTC2624 quad DAC to achieve fine output. As the DAC output is very fine so LPF is not needed. Hence it requires less space on chip. We have implemented a 12-bit DDS by using only 128 memory location in spite of using 4096 memory locations hence only 3% memory is used. Phase accumulator is the heart of the system [10]. The contents of Frequency Control Word register (FCW) is added to phase register at each clock cycle. Hence phase accumulator is to be considered as a digital phase wheel [10]. Output of phase accumulator is fed to the Look Up Table to generate a complete sinusoidal waveform.

Direct digital synthesizer can generate waveform of desired frequency just by changing the contents of Frequency control word register (FCW). This relation can be shown by (1)

$$F_{out} = (M * f_{clk}) / 2^n \quad (1)$$

Where M, fclk and n are FCW, clock frequency and width of accumulator respectively.

Phase of sine wave depends upon clock frequency. A small phase change Δp is expressed by

$$\Delta p = \omega . \Delta t \quad (2)$$

Where Δp, ω and Δt are phase change, angular frequency and small change of time of sine wave respectively. By (3) we get

$$\omega = \Delta p/\Delta t = 2\pi f \quad (3)$$

II. Proposed Architecture

In proposed architecture we have implemented a 12-bit DDS, which uses phase truncation and quadrature symmetry to reduce memory. We have used phase dithering [5] to reduce the amplitude errors generated due to phase truncation. Fig. 1 shows the block schematic of system. The complete design is implemented on SPARTAN 3E FPGA, which uses LTC2624 quad DAC.

Phase accumulator is the heart of the system. It works as a digital phase wheel [10]. By changing contents of Frequency Control Word Register (FCW), we can change the output frequency. As length of accumulator increases, system's speed increases too. We have used phase truncation [5], quadrature symmetry of sine wave [6] and phase dithering [5] to reduce memory. The output of phase accumulator is fed to look up table and output of look up table is fed to the DAC.

A. Phase truncation

In this we have truncated last 4 LSBs because last LSBs contain least amount of information. By truncating last required memory will be 2^{n-3}.

B. Quadrature symmetry of sine function

As we know that sine wave has quarter symmetry. So if we use only first half of quarter cycle than whole sine wave can be constructed without any error compensation.

C. Phase dither

In phase dithering we add 3 or 4 bit random number at the output of phase accumulator so that the amplitude errors generated by phase truncation can be compensated.

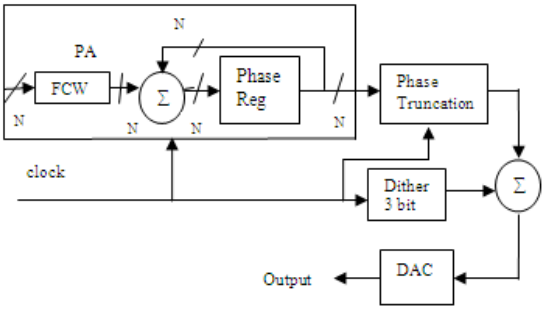

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Figure 1. Proposed architecture (using dither).

D. *Effect of frequency control word*

Fig.4 shows the effect of FCW on output frequency.

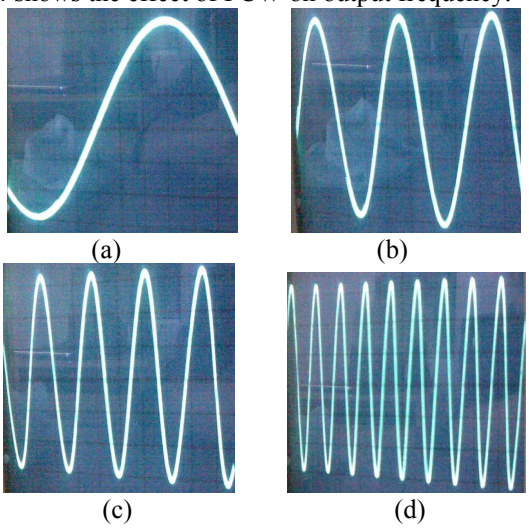

Figure 2. Effect of frequency control word (FCW) on output frequency.

Fig. 4 (a-d) shows output waveform at FCW= 2, 5, 10 & 20 respectively. Table I lists the effect of FCW. As we have seen that the output frequency increases in multiples of FCW.

E. *Effect of quadrature symmetry of sine function*

Table II lists the effect of quadrature symmetry.

F. *Effect of phase truncation*

Fig. 5 (a-d) shows the effect of phase truncation. Due to phase truncation some amplitude errors are generated.

G. *Effect of phase dither*

Fig. 4 (a-d) shows the effect of phase dither. Amplitude errors are reduced.

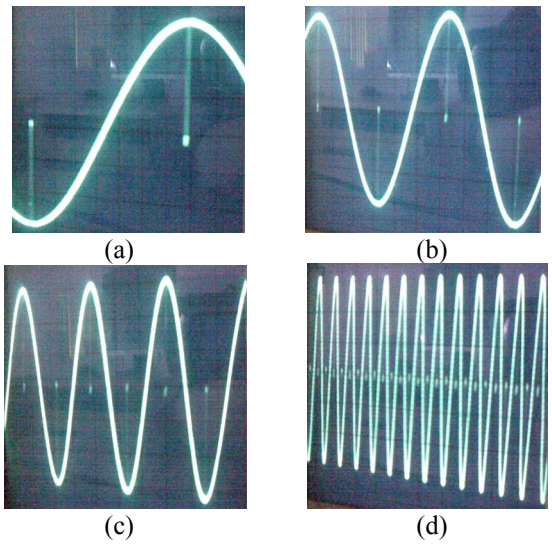

Figure 3. Effect of phase truncation.

TABLE I. EFFECT OF FREQUENCY CONTROL WORD

Frequency Control Word (FCW)	OUTPUT FREQUENCY (KHZ)
1	2
2	36.62
5	61.03
10	122
20	244.14
50	610.035

TABLE II. EFFECT OF QUADRATURE SYMMETRY OF SINE FUNCTION

DDS Model 12-bit	MEMORY LOCATIONS REQUIRED
Simple DDS	4096
Phase truncation	512
Quadrature symmetry	1024
Proposed work	128

III. CONCLUSION

The FPGA based design of DDS has been successfully implemented on XILINX Spartan 3E board. Simulations has been done using XILINX ISE 8.1i and ModelSim XE III 6.c.

As the accumulator length increases, ROM size increases also. Hence to reduce memory phase truncation and quadrature symmetry have been employed. To reduce errors generated by phase truncation, a phase dithering model also has been proposed.

In our design we have implemented a 12 bit DDS on FPGA. But we can implement a DDS of any accumulator size just by changing the size of phase accumulator. This design is very useful in biomedical function generator because it generates a very accurate and fine waveform of desired frequency. This design can also be used in military applications like RADAR. Further more memory can also be reduced by increasing phase truncation.

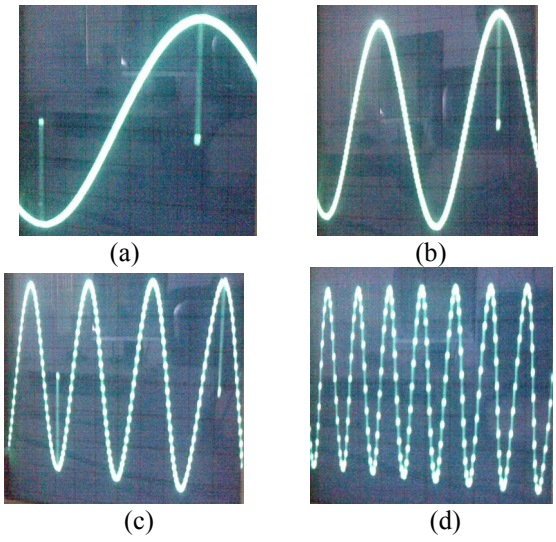

Figure 4. Effect of phase dithering.

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REFERENCES

[1] J. Tierney, C.M.Radre, and B. Gold , “A Digital Frequency Synthesizer”, IEEE Transactions on Audio and Electroacoustic, vol Au 19, No.1, pp. 48-57, March 1971.

[2] H. T. NicholasIII, H.Samueli and B.Kim, "The Optimization Of Direct Digital Frequency Synthesizer Performance In The Presence Of Finite Word Length Effects", 42nd Annul.

[3] Paul O. Leary and Franco Maloborti, "A Direct Digital Synthesizer With Improoved Spectral Performances", IEEE Trans. On Communication, Vol. 39, No.7, pp. 1046-1048, July 1991.

[4] Jose M. Riera Salis, "Spurious Performance of Direct Digital Synthesizers Generating Modulated Signals", IEEE electrotechnical conference, Vol.1, pp. 223-226, April 1994.

[5] H.T. Nicholas and H. Samueli, " An Analysis Of Output Spectrum Of Direct Digital Frequency Synthesizer In The Presence Of Phase Accumulator Truncation", Proceedings of the 41st IEEE Annual Frequency Control Symposium, pp. 495-502, 1987.

[6] John N. Lygouras, "Memory Reduction in Look-Up Tables for Fast Symmetric Function Generators", IEEE Transactions On Instrumentation And Measurement, Vol. 48, No. 6, pp. 1254-1258, December 1999.

[7] Zhang Shaoyuan, Yao Fuquiang, Zhang Shuoao, "Spur Reduction For DDS Phase Accumulators", IEEE, pp. 189-193, 2001.

[8] Sunita Khilar, Kiran Parmar, Saumi S, Dr. K.S. Dasgupta, "Design and analysis of direct digital frequency synthesizer", IEEE conference on emerging trends in engg. And tech., pp. 1302-1306, Aug 2008.

[9] "Spartan 3E Starter Kit User Guide", UG 230, V1.0, Xilinx User Guide,pp.67-71, March 2006.

[10] Jouko Vankka, "Direct Digital Synthesizers: Theory, Design and Applications", Boston ; London : Kluwer Academic Publishers, 2001.

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