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CAD Design of Operational Amplifiers with Noise Power Balance for SoC Application

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Abstract-- **Advances in integrated circuit technology have led to the birth and proliferation of a wide variety of integrated circuits, including but not limited to application specific integrated circuits(ASIC), various types of microcontrollers and processors. Many applications such as communication devices (VoIP, MoIP, wireless) require chip speeds that may be unattainable with separate IC products. Creating portable analog modules requires the system to capture not only the sized schematic of the circuit but also the objectives that circuit is trying to achieved.This paper applies the embedding knowledge into pure simulation based methodology to perform automatic analog intergraded circuit design, synthesis and optimization in order to reduce development time of this kind of circuits. A practical platform independent computer aided design methodology for synthesis of (analog circuits) Operational Amplifier with flexible noise –power balance is presented in this paper. In order to evaluate the fitness of the circuit specifications in any iteration of SA, NGSPICE simulation is used. The simulation results confirm the efficiency of presented methodology in determining the device sizes in analog circuits.**

Index Terms—**Analog circuit designs methodologies, Analog design automation, ASIC, CAD, EDA tools, Op-amps, Simulated Annealing, SPICE, SoC, AMS.**

I. Introduction

In recent years, there have been great advancements in the speed, power, and complexity of integrated circuits; such as application specific integrated circuit (ASIC) chips. ASIC technology has evolved from a chip-set philosophy to an embedded core based system-on-a-chip (SoC) i.e. analog and mixed signal (AMS) chip concept. Many applications such as communication devices (VoIP, MoIP, wireless) require chip speeds that may be unattainable with separate IC products. The term "system-on-chip" may be used to describe many of today's complex ASICs, where many functions previously achieved by combining multiple chips on a board are now provided by one single chip, these advancements have made possible the development of system-on-a-chip (SOC) devices.

System on a chip (SOC) is used in a wide variety of electronic equipment, including portable or handheld, devices. Such handheld devices include personal digital assistants (PDA), CD players, MP3 players, DVD players, AM/FM radio, a pager, cellular phones, etc. Such electronic technologies have facilitated increased productivity and reduced costs in a number of activities, including the analysis and communication of data, ideas and trends in most areas of business, science, education and entertainment. SOC products provide faster chip speeds due to the integration of the components/functions into one chip. Many applications such as high-speed communication devices require chip speeds that may be unattainable with separate IC products [1].The reduction in size afforded by SOCs also leads to improvements in power consumption and device speed. Circuit operations that occur on a single integrated circuit require much less power than a similar circuit implemented on a PCB with discrete components. For example, a SoC for a cellular telephone.

In AMS chips the most of the successful analog designs are carried out by expertise which is dependent on their knowledge and experience. Considering the trend of integrating millions of transistors on a chip, this is not feasible to rely on full-custom designed blocks. Therefore, it is extremely difficult for a novice designer to do high-performance analog and mixed-signal (AMS) design. Analog design automation is also motivated to reduce design and productivity gap. The formal verification of AMS design is relatively young research field and still under developed [2].

The market tends towards mixed signal chips demands equal pace for both digital and analog sections. To meet these constraints designers must reuse proven design and leverage them as building block of the new design. This kind of design tools are well established in digital circuits [3] [4]. However same can not be said about analog circuits, lacks consistent design methods [3]. Therefore developing reliable automatic tool in analog IC design seems very challenging as well as attractive task.

In this study we used, Simulated Annealing (SA) [5] Algorithm as a global optimum search engine. The simulated annealing (SA) algorithm is an effective tool in the field of VLSI computer-aided design. This stems from both its general applicability to a wide range of combinatorial optimization problems and that it consistently produces high quality solutions for these problems. With SA, NGSPICE [6] as the fitness evaluator, two stage operational amplifier is optimized as an example analog device. Optimization characteristics include DC bias and frequency domain characteristics and noise analysis.

The previous approaches used for analog automation which are either purely knowledge based or optimization based [7-12] tends to increase design time and sometimes

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have convergence problem also. The presented methodology is more accurate, general, flexible and less time consuming.

II. Frame Work

The most often used analog building block is the operational amplifiers (Op-amps). It is at the heart of many interface circuits, like Analog to Digital converters, Filters, etc. An efficient design of optimal Op-amps is thus a cornerstone of a design environment of many applications. Designing good Op-amps is a rather complicated multifaceted task.

The two stage amplifier Opamp shown in Figure 1 is one of the design examples of such circuits. It provides high gain and high output swing and is very suitable for low voltage applications where few transistors can be stacked to provide sufficient gain.

The Opamp is optimized for the DC gain, unity- gain bandwidth phase margin, minimum area, CMRR with flexible power balance scheme. Keeping these parameters as objective goals the fitness parameters are defined to meet constraints.

In this problem unknown parameters are W and L of all MOS transistors. Some of the W 's and L 's equal. (For example $W1 = W2$). While designing individual sub blocks basic analytical equations are used to decide the range of W 's and L 's. This helps search engine lesser convergence time.

$$L_{min} <= L_i <= L_{max}$$

$$W_{min} <= W_j <= W_{max}$$

Where value of i , j varies as per sub circuit design. Since sub circuits are simple to design, it does not require complex calculations and can be easily done [13]. For the two stage operational amplifiers shown in Figure 1 the value of C_L =1 pf and V_{DD} = ± 2.5V kept constant.

III. Novel Design Methodology

The embedded knowledge based design methodology is modification of pure simulation based approach. Here, some basic knowledge about the circuit, as a set of analog design rules, is incorporated into the search mechanism. This guides the search engine towards solution in much faster times. It is also process independent and designer doesn't need to have expert knowledge about the in- depth working circuit. No complex equations and models need to be written and solved to obtain the solution. This technique leads to global optimal synthesis solution for fixed topology. Simulated Annealing (SA) Algorithm is used as a global optimum search engine.

The first phase of the design methodology is hierarchical circuit partitioning. A two-stage Op-amps topology we used is shown in Figure1. It can be partitioned into following sub circuits. A Difference Amplifier, A Gain Amplifier, A Current Mirror circuit and Feedback network. Such a structural partitioning results in hierarchical view of the Op-amps circuit described in figure 2 and then the design represented in electronic format.

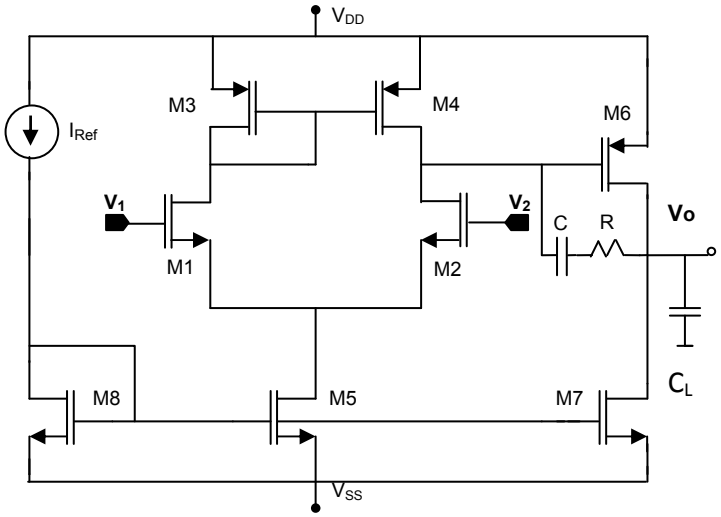

Figure 1. Two-Stage Operational Amplifiers

The second phase in the methodology is the design synthesis phase. Hierarchically partitioned sub-circuits are designed for specifications derived using a knowledge-based methodology, such as circuit analysis for the sub circuit or heuristics. For example: The MOSFETS are main component of all sub circuit During the circuit optimization phase, the CMOS transistor is modeled as a four terminal device with the terminals drain, gate, source and bulk. Given the potentials at the terminals the drain current, threshold voltage, saturation voltages are computed according to the transistor model. After sub circuits are designed, the circuit is converted into a flat circuit net list. I.e. spice netlist for considered analog circuit. The flat net list then simulated using an analog simulator such as NGSPICE [6]. If the obtained result is not near to the target specification cost of the circuit, then at least one of the sub-circuits or component redesigned with another set of design specifications for the topology.

The design procedure mentioned [7] assuming perfect square-law MOS modeling, we can expect some nonlinear distortion of the output signal due to the second order effects. These effects are mobility reduction, channel-length

modulation and the body effect. The first two of them are process dependent. That means as the process changes the all the design steps required to be derived again. Since methodology presented in this paper is process independent it avoids complex algebraic equation solving. At the same time [7] it does not take into account 1/f noise contribution while calculation of Noise spectral density.

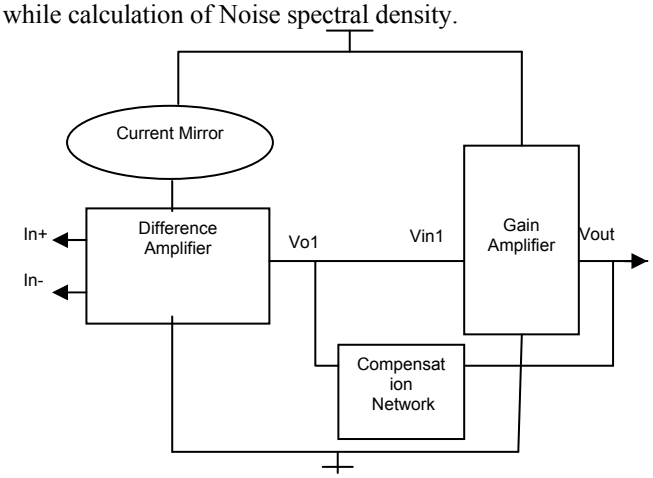

Figure 2. Structural Partitioned Hierarchical Blocks of Op-amps

The suggested CAD design methodology algorithm for analog circuit is as follows

Step1: Select the topology.

Step2: Initial value selection for width (W) and Length (L) for each transistor in the circuit.

Step3: Create Spice Netlist of the selected topology.

Step4: Create Spice test bench for simulation.

Step5: Read spice output in text form.

Step6: Extract the parameters like bandwidth, gain etc

Step7: Repeat step 4 to 6 for extracting different parameters

Step8: Calculate the cost function.

Step9: If achieved results are better than spaces then design is done.

Step10: If achieved results are not better than spaces then the select another set of values for width and length and repeat step 3 onwards till design is done.

IV. Cost Function

Simulated annealing [5] is optimation method applicable for searching for global minimum of cost function. It is objective of the algorithm to maximize the fitness of specifications subject to hard constraints that exits within the system. The cost mapping function evaluates the relative fitness of particular solution specification. It is this process that derives the heuristic algorithm towards better solution. The cost mapping function takes the many different objectives into account. The fitness value of specifications is a subject measure of device performance. In this work, the cost function defined as weighted sum performance parameters of the circuit. For synthesis of the two stage Operational amplifiers the cost function is weighted sum of the gain of Op-amps, bandwidth, area, etc and can be represented as

$$\cos t = k\sum_{i=1}^{n} w_i * f_i$$

Where

k = constant $0< k <1$

w_i =assigned weight coefficient of performance parameter i

f_i =desired value determined for performance parameter i

n = Number of performance parameters.

V. Synthesis Procedure

We synthesized the two stage Operational Amplifiers using the suggested methodology. The implementation of methodology is done using standard Perl. The source code consists of more than 1000 lines. The code was complied on a PC with Intel Core 2 Duo processor at 2.1 GHz, (3.5GB RAM). The values of W 's and L 's for the different MOS transistors are changed randomly during synthesis process.

The Op-amps specifications used are [7]

- Required gain Ad > 80db
- Gain Bandwidth Product >= 5MHz
- Swing >2V
- Phase margin > 65 degree
- Area = Minimum
- CMRR = 70db
- Power =Minimum

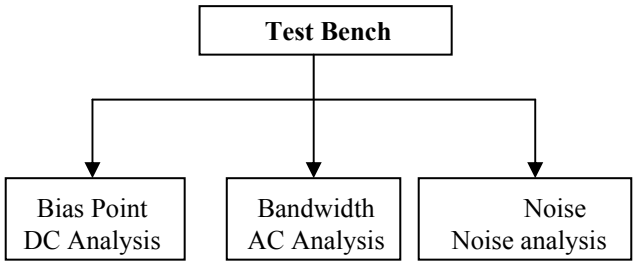

Figure3. Different test bench incorporated in CAD Design methodology

The first parameter can be directly measured by AC analysis in ngSpice. The noise analysis is done using onoise spectrum analysis in ngSpice. The different DC bais voltages and currents are is calculated using DC analysis in ngSpice. All this parameters are generated using appropriate test bench analysis (Figure 3) which is incorporated in flat net list as per analysis type. The generated flat net list is run in spice batch mode to compare the results with given constraints list. The spice net list is simulated using BSIM3V3, Level49 model.

The first four parameters can be directly measured by AC analysis in ngSpice.

For remaining parameter analytic equation are incorporated in the program.

The analytical equations are shown below.

$$Area = \alpha_0 + \alpha_1 * c_c + \alpha_2 \sum_{i=1}^{n} W_i * L_i$$

where,

n = Number of Mosfet

$Area$ in μm^2, $\alpha_0 \geq 0$ gives fixed area, α_1 is the ratio of capacitor area to capacitance and the constant $\alpha_2 \geq 1$(if

it is not one) [12]. The area calculation varies as per layout rule.

$$CMRR = 20 * \log_{10}\left(Ad/Ac\right)$$

where,

$CMRR$ =Common mode rejection ratio

Ad = differential gain,

Ac = Common mode gain

VI. Design Example

The design example is provided to illustrate the use of methodology. Following the synthesis procedure for the proposed methodology in section V, the transistor sizing for schematic in Figure 1 with Cc =2.5 pf is provided in table 4. As seen from table 5, the proposed design methodology provided the better results than the obtained values in [7], [15] except DC gain Ad . Using our methodology the resulted value of DC gain Ad proven be correct when compare with analytic equation [14]. The obtained onoise spectrum response of the designed two Stage Operational Amplifiers with Cc =2.5 pf is shown in the Figure 6.

The flexibility and efficiency of the proposed methodology demonstrated by designing and transistor sizing for schematic in Figure 1 with Cc =0.5 pf. The results are provided in table7. As seen from table 8, the proposed design methodology provided the much better gain bandwidth product than the obtained values in [7], [15] but less DC gain Ad . The obtained onoise spectrum response of the designed two Stage Operational Amplifier with Cc =0.5 pf is shown in Figure 9 and the frequency response is shown in Figure10. The obtained value of noise spectrum in Table5and 8are larger than then [7] and [15] since we have taken into account 1/f noise contribution while calculation of Noise spectral density.

TABLE 4. The Sized Circuit Components with CC =2.5 pf

For Cc =2.5 pf		
	Dimensions	Unit
$(W/L)_{1,2}$	2/0.5	µm/ µm
$(W/L)_{3,4}$	4/0.4	µm/ µm
$(W/L)_{5,8}$	1.5/1	µm/ µm
$(W/L)_{6}$	110/4.5	µm/ µm
$(W/L)_{7}$	4.5/1	µm/ µm
$(W/L)_{9}$	10/1	µm/ µm

TABLE 5. The Comparative Results with CC =2.5 pf

Parameters	Obtained Value by[15]	Obtained Value by[7]	Obtained Value by proposed methodology	Unit
Power	367	394	108	µ W
Gain	83.9	83.1	76.774	Db
Phase margin	66	65	67	Degree
Swing	2.2/-2.2	2.16/-2.2	2.2/-2.1	V
Gain BW	5	5.44	5.46	MHz
Area	1040	1220	860	μm^2
CMRR	-	-	72	Db
noise@1 Mhz	21	18	28.18	$nV/\sqrt{Hz}$

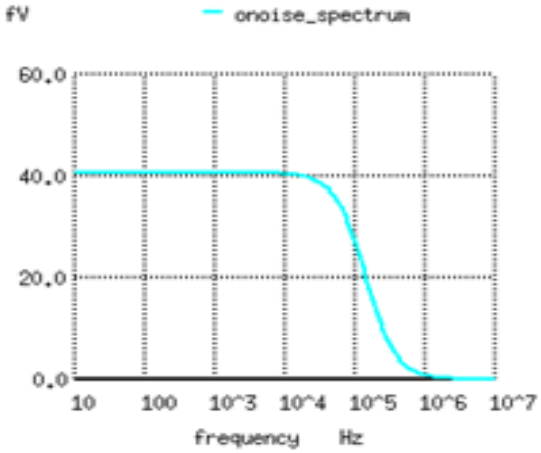

Figure 6. The obtained Onoise spectrum response of Two Stage Operational Amplifers with Cc =2.5 pf

For Cc =0.5 pf		
	Dimensions	Unit
$(W/L)_{1,2}$	0.2/025	µm/ µm
$(W/L)_{3,4}$	1/1	µm/ µm
$(W/L)_{5,8}$	1/3	µm/ µm
$(W/L)_{6}$	31/2.5	µm/ µm
$(W/L)_{7}$	3/1	µm/ µm
$(W/L)_{9}$	1/2	µm/ µm

TABLE7. The Sized Circuit Components with CC =0.5 pf

Parameters	Obtained Value by[15]	Obtained Value by[7]	Obtained Value by proposed methodology	Unit
Power	207	207	102	µ W
Gain	85.4	85.1	39.61	Db
Phase margin	46	65	60	Degree
Swing	2.3/-2.25	2.16/-2.2	2.12/-2.1	V
Gain BW	4.79	6.0	12.03	MHz
Area	571	234	180	μm^2
CMRR	-	-	70	Db

noise@1 Mhz	44	38	79.26	$nV/\sqrt{Hz}$

TABLE 8. THE COMPARATIVE RESULTS WITH CC =0.5 pf

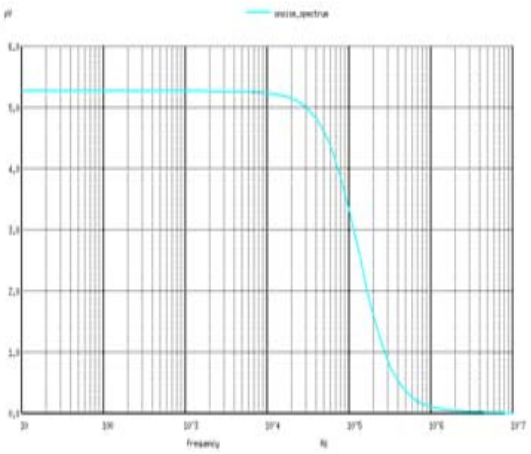

Figure9. The obtained Onoise spectrum response of Two Stage Operational Amplifiers with Cc =0.5 pf

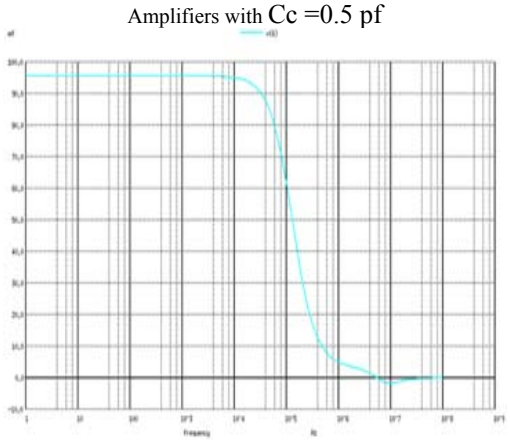

Figure10. The obtained frequency response of Two Stage Operational Amplifiers with Cc =0.5 pf

VII. CONCLUSION AND FUTURE SCOPE

A practical CAD design methodology for synthesis of two stage Amplifiers with noise power balance scheme is presented in this paper. It involved embedded knowledge into pure simulation based methodology without any intervention from expert designers. The methodology avoids the in depth circuit analysis of large circuits and formulating design equations for large circuits. Instead, the designers have to analyze and formulate the design equations for smaller sub circuits. This is expected to save significant design time and efforts.

Experimental results show that the analog design rules in the used methodology, guide the search engine in producing constraint satisfying solution, in very short times. The obtained results listed in table 5 and table 8 achieve better than [7] [[15].The synthesis tool is technology independent and can be used for synthesis of wide variety of analog circuits and topologies.

In order to accommodate other user-defined constraints, no changes in the design flow are necessary. Only the cost function is required to be modified to incorporate the new constraints which can be easily done. In near future we will try to explore robustness of the CAD tool with various analog circuit designs like Transconductance multipliers, Analog to digital converter, voltage controlled oscillator (VCO) .

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