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Design of a Digital Preprocessor System Based on Software Radios Conception

Dingkun Ma, Xiaomin Zhang and Jian Luo

***Abstract*—the paper designs and implements a six-channel digital preprocessor system. The preprocessor system is designed as much digital structure as possible, by calling the corresponding software packages, the basic hardware parameters of preprocessor system can be adjust to meet different needs in specific applications. Compared with the conventional preprocessor circuits, the digital preprocessor system has virtues of high sensitivity, low power consumption, standardization and software-based, more over, it is capable of network building. The digital preprocessor system has been applied in a target detection system, the experiment results show that the method is very promising.**

***Index Terms*—digital preprocessor system; software packages; digital AGC; Intelligent Communication Node**

I. Introduction

The conventional signal preprocessor circuits consist of fixed-gain amplifier circuits, fixed-bandwidth filters and analog AGC circuits, it could only meet the requirements of specific application generally. With the developing of the new digital signal detection algorithm and structure, In order to detect weak signal in complex and changeable background, it raises higher requirements for signal preprocessor system designing [1]. U.S. scientist Joe Mitola set forth the concept of software radios clearly at telecommunications meeting for the first time [2, 3], bringing inspiration to the design work of preprocessor system. In the process preprocessor system design, by introducing the idea of software radios, the versatility and flexibility of the preprocessor system should be fully considered, the hardware parameters of the preprocessor system should be set by software conveniently. With the support of proper sensors, software packages and programmable preprocessor system, the digital preprocessor system could meet the requirements of corresponding application. Designers only need give thought to how to combine the software packages, preprocessor system can be programmed to satisfy the specific requirements of detection.

II. Design Scheme

The design work of digital preprocessor system is based on low-power techniques to meet the requirements of long-term battery-powered applications. To detect weak signals, the preamplifier of preprocessor circuit adopts a special design structure to reduce the preprocessor system's self-noise greatly. The controller adopts TI's 16-bit Micro-Power MCU MSP430F5438, which is in charge of the whole control tasks of digital preprocessor system. The preprocessor system is composed of six channels, according to the specific needs of different applications, certain channels could be switched on to work, and other redundant channels could be switched off to reduce power consumption by software. Each channel of the preprocessor system is composed of pre-amplifier, programmable band-pass filter, digital AGC and intelligent bus node, the structural diagram of preprocessor system is as shown in Figure 1.

In order to reduce preprocessor system power consumption, the preprocessor system has always switched one channel on to work as watching function, the MCU would switch on the other independent channels to accomplish further detection as soon as it detect suspicious target. Working band and gain of each channel could be adjusted continuously and independently according to the signal in specific application, Digital

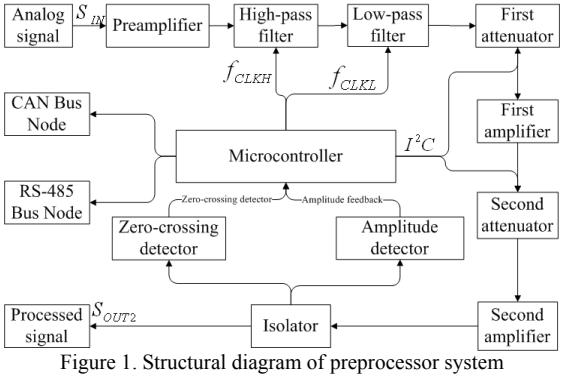

Figure 1. Structural diagram of preprocessor system

AGC techniques have been introduced into preprocessor system, when the non-predictable inferences modulate amplitude of input signal in a large range, the amplitude of output signal could always keep stable. Meanwhile, the preprocessor system adopts the combination of CAN bus and RS-485 bus to facilitate information sharing and controlling among modules by bus interconnect and standard communication protocols.

III. Hardware Design

The hardware design of preprocessor system is based on the principles of low self-noise and low power consumption, most important of all, it should also be programmable.

A. Design of Pre-amplifier

The mission of preprocessor system is to detect weak signal, the performance of pre-amplifier is key to

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preprocessor system's noise indicator. The preprocessor system adopt low-noise transistor 3DM3C as pre-amplification, schematic diagram is as shown in figure 2. A bootstrap structure is used in the bias system to improve input impedance and reduce self-noise of the preprocessor system at the same time.

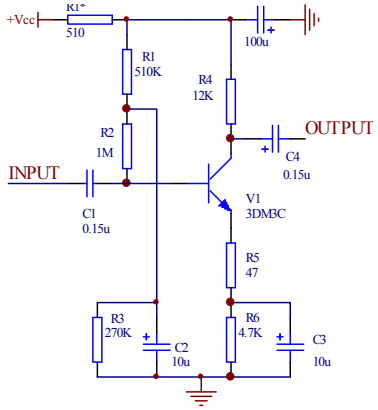


Figure2. Pre-amplifier schematic diagram

The gain of pre-amplifier could be adjusted according as the formula (1)

$$A_g = R4 / R5 \qquad (1)$$

B. Design of Band-Pass Filter

The power consumption of band-pass filer is critical to low-power design of the preprocessor system, upper and lower cut-off frequency of filter should be adjusted by software continuously. As a result, Linear's universal switched-capacitor filter LTC1068 and Maxim's lowpass filter MAX7414 are chose as high-pass and low-pass filter respectively. LTC1068 is composed of four identical 2nd order filter sections, the function type of filter can be easily defined through external resistors, the operating supply current is only 3.2mA when LTC1068 is powered by 3V[4]. Meanwhile, MAX7414 is a 5th-order, switched-capacitor filter which has Butterworth response, it consumes only 1.2mA when MAX7414 is powered by ±3V[5].

The cut-off frequency of high-pass hand low-pass filter can be set by external programmed clock signal. In order to reduce the power consumption of band-pass filter section, LTC1068 is split into two four order filter for two channels of preprocessor system, and programmed as elliptic high-pass filter to get a steep transition band by external resistors, schematic diagram of the band-pass filter is as shown in figure 3.

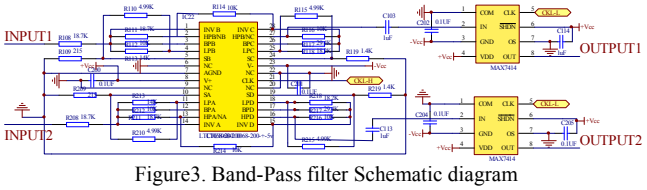


Figure3. Band-Pass filter Schematic diagram

When band-pass filter is powered by ± 3V supply in test, the working current consumption is only 3mA per channel.

C. Design of Zero-crossing Detector

The module's mission is to realize watching function of system. Zero-crossing detector make a bit quantization for the input signal, it is a digital processing system with no A/D essentially. Zero-crossing detector makes use of the amplifier saturation principle. Timer module built in MCU counts the times of signal's zero-crossing in a second for suspect signal prediction. As soon as the preprocessor system detects suspicious signal, it would wake other channels to accomplish further intelligent detection with multiple-channel signals.

D. Design of Digital AGC

The design of PGA is important to digital AGC implementation, preprocessor system adopt fixed-gain amplifier cascading digital potentiometer attenuator as PGA architecture. The attenuator adopts Xicor's X9268, which provides I^2C serial interface to set wiper position to adjust the gain of PGA conveniently [6]. The receiver monitors aptitude of output signal, and sets PGA by software to output a smooth signal in spite of input swinging.

E. Design of Communication Node

Preprocessor system collaborates with other modules by the combination of CAN and RS-485 bus. Simple control instructions can be transmitted by RS-485, while CAN bus is responsible for the transmission of large mount of data. Based on the consideration of low-power design techniques, preprocessor system adopts Microchip's MCP2515CAN with SPI serial interface as transceiver of CAN bus, its standby current is only 10μA/5.5V, Maxim's MAX3485 is used as controller of RS-485 bus, standby current of which is only 20nA, schematic diagram of the CAN bus node is as shown in figure 4.

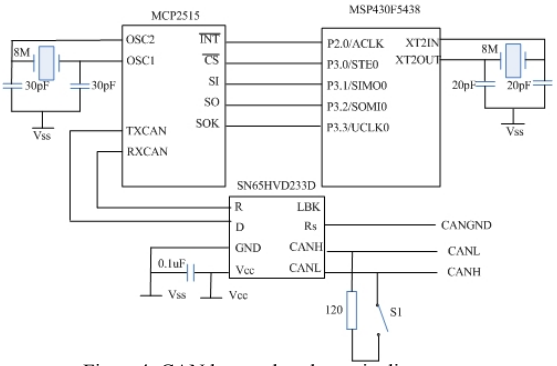


Figure4. CAN bus node schematic diagram

IV. Design of Software

Compared with traditional analog preprocessor system, being programmable is the biggest of virtue of digital preprocessor system. Supported by the programmed design, the hardware parameters of preprocessor system could be defined by calling corresponding software packages. All the controlling tasks are accomplished by MSP430F5438, it includes the selection of channel, the setting of working band, digital AGC algorithm, zero-crossing detection, intelligent communications nodes, and the preprocessor system control block diagram is as shown in figure 5.

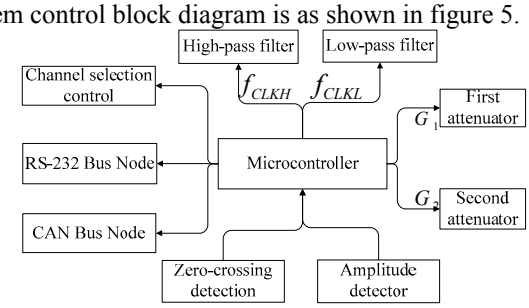


Figure5. Control function diagram of the preprocessor system

A. Software Design of Channel and Working Band Selection

Microcontroller outputs high level or low level to control analog switch ADG452, and selects the working channel by performing the action of power-on or power-down, the operating band of preprocessor system can be set by timer module, which outputs programmed clock signal to set cut-off frequency of the filter, so that the operating band of preprocessor system could cover the frequency range of signal.

B. Software Design of Digital AGC Algorithm

In order to compress the dynamic range of signal's amplitude, AGC should obtain the current amplitude of signal firstly. The algorithm adopts a method of counting times of signal passing fixed-threshold in a second to improve the flexibility of amplitude extraction. The preprocessor system samples signal with A/D and counts the times of signal passing fixed-threshold, software looks up the amplitude C(i) of signal from a reference table, and accomplishes the extraction of signal amplitude. Assuming that the counting times of processed signal by AGC is C, the subtraction of C(i) and C are used as the input for PID controller, the PID algorithm with feature of dead-zone and integral separation is introduced into AGC, the PID output is used to adjust PGA to realize digital AGC, which would stabilize the amplitude of output signal timely with high accuracy. The basic PID algorithm is as follows:

$$\Delta u(k) = K_p[e(k) - e(k-1)] + K_i e(k) + K_d[e(k) - 2e(k-1) + e(k-2)] \quad (2)$$

In the process of AGC adjustment, the physical meaning of PID parameters are as follow, $e(k)$ is subtraction of C(i) and C at k moment, $\Delta u(k)$ is the step of PGA adjustment [1]. Digital AGC control algorithm flowchart is as shown in Figure 6.

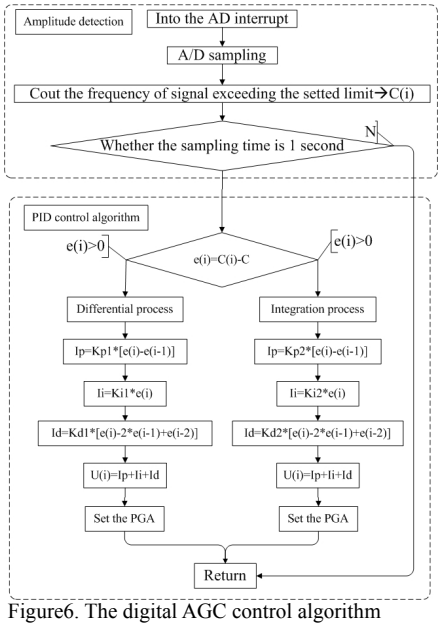


Figure6. The digital AGC control algorithm

In analog AGC, different effects of AGC control can only be realized by changing hardware such as different resistances and capacitances, the hardware configuration must be changed to fit the requirements of different applications. In the PID algorithm, two different sets of PID coefficients are adopted according to the value of e(i), which is corresponding to different charge and discharge constant in analog AGC. The preprocessor system could achieve different effects of AGC controlling by setting appropriate control coefficient in software, and change the way of AGC debugging. More over, the steady-state attenuation value of AGC can be read easily in digital AGC to meet requirements of quantitative of energy detection in some specific applications.

C. Watching Detection Algorithm

In order to reduce the power consumption of preprocessor system, only one channel is always working as watching detection, other channels is in sleep mode usually.

The watching detection is to monitor the changes of acoustic signal which is radiated by the target, so that it could forecast the emergence of target. The system calculates the zero-crossing times of band-limited acoustic signal in a second, the mean times is relevant to power spectral density of the signal, but not sensitive to the changes of signal's amplitude. When a target approaches the preprocessor system, and brings a new power spectral component, the times of zero-crossing will changed. This feature is suited well for forecasting appearing of line spectrum and monitoring changes of signal power spectrum continually [7].

Rice.S.O deduces academic relationship between the mean zero-crossing of stationary Gauss noise and its power spectral density for the first time [10].

$$A = 2[\int_0^\infty f^2 W(f)df / \int_0^\infty W(f)df]^{\frac{1}{2}} \quad (3)$$

In the formula, A is the mean zero-crossing times of noise, $W(f)$ is the noise's power spectral density function.

In order to validate the conclusion before, we study the condition that line spectrum hides in the background of band-limited white noise, line spectrum component is corresponding with sine wave in the time domain theoretically, so the power spectral density of line spectrum component and the noise in the background is as follow:

$$W_1(f) = \begin{cases} r(f_H - f_L) & When: f = f_S \\ 0 & When: f = others \end{cases} \quad (4)$$

$$W_2(f) = \begin{cases} 1 & When: f_L < f \le f_H \\ 0 & When: f = others \end{cases} \quad (5)$$

In the formula, f_S is the frequency of line spectrum component, r is the ratio between line spectrum and band-limited continuous spectrum of noise, it is also called signal noise ratio(SNR). The summation of line spectrum and Gauss noise power spectrum density is:

$$W(f) = W_1(f) + W_2(f) \quad (6)$$

The mean times if signal's zero-crossing educed by (3) is:

$$A = 2[\frac{\frac{1}{3}(f_L^2 + f_L f_H + f_H^2) + r f_S^2}{1+r}]^{\frac{1}{2}} \quad (7)$$

The mean times of zero-crossing are based Stat. of long sample. The zero-crossing times of the noise radiated by target and noise in background trend to gauss distribute, and both is A. The conclusion is consistent with 'central limit theorem'.

As the component of noise in the background is time-varying, the mean zero-crossing times of signal is not stable, zero-crossing detection algorism in time-varying background is as shown in figure 7.

The confidence interval of automatic threshold is brought into zero-crossing detection algorism, and it has upper confidence limit and lower confidence limit respectively.

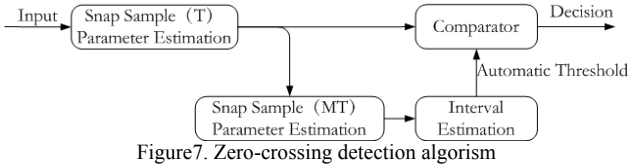


Figure7. Zero-crossing detection algorism

$$1-\alpha = P\left\{\bar{X} - \frac{S}{\sqrt{N}} t_{\alpha/2} \le \mu < \bar{X} + \frac{S}{\sqrt{N}} t_{\alpha/2}\right\} \quad (8)$$

The upper threshold and lower threshold defined in confidence interval is as follow:

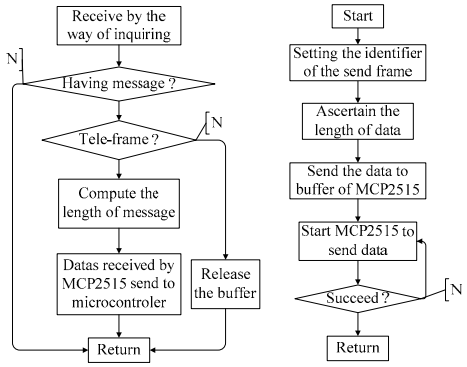
$$A_T = \bar{X} - \frac{S}{\sqrt{N}} t_{\alpha/2} \quad \text{(Upper threshold)}$$

$$A_T = \bar{X} + \frac{S}{\sqrt{N}} t_{\alpha/2} \quad \text{(Lower threshold)}$$

The false alarm probability that mean zero-crossing times fall out of the upper threshold and lower threshold is α .When high frequency or low frequency of line spectrum appears in the input spectrum, the mean times would fall into the threshold, the preprocessor system would alarm that the target is coming near of leaving out.

D. Software Design of Intelligent Communication Node

Software design of intelligent communication node includes CAN and RS-485 serial bus。RS-485 could be realized by URAT module integrated in the MSP430F5438, software only needs to define its own control word. The mission CAN should accomplish is to transmit the data to other nodes, and receive data from bus, the flow chart of CAN bus is as shown in figure 8.



Flow Chart of Message Receiving Flow Chart of Message Sending

Figure8. CAN bus flow chart

V. Technical Parameters of Preprocessor System

A. Power Consumption Test

When the preprocessor system is powered by ±3V, the operating current is 8.5 mA per channel.

B. Preprocessor system Sensitivity

The preprocessor system‘s equivalent input noise is $0.0918\,uV$ on the condition that the input circuit is short.

C. Working Band Tests

The band-pass filter of preprocessor system is composed of high-pass and low-pass filter, its upper and lower cut-off frequency could be adjusted continuous by software over a range of 10Hz-30 kHz. In the test, the band-pass filter is programmed as [1 kHz 5 kHz], the amplitude-frequency of band-pass filter response curve is as shown in figure 9, the attenuation in transition zone is greater than 30dB, and the flatness of pass-band is less than 1 dB.

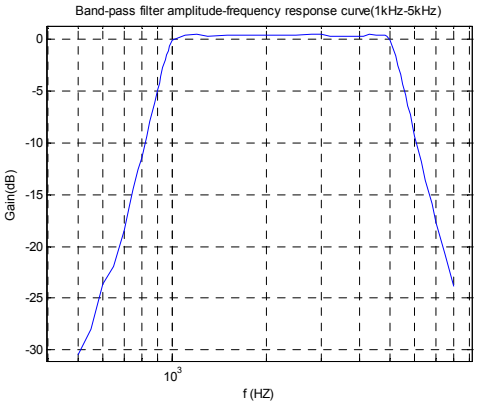


Figure9. Band-pass filter amplitude-frequency response curve

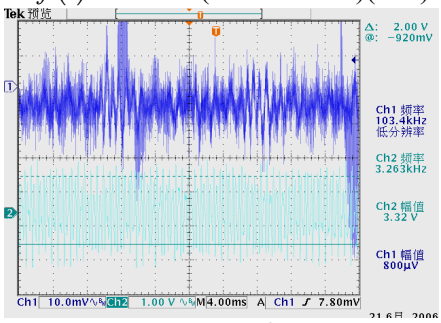
D. Digital AGC Control Test

when the input of the *preprocessor system* is a sine signal:

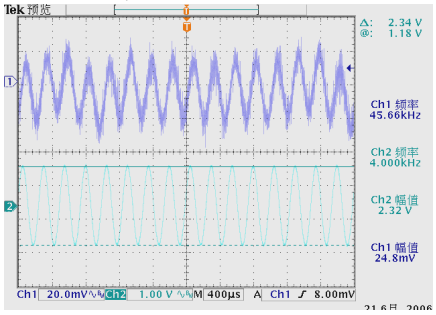
$$f(t) = 0.1 \times \sin(2 \times \pi \times 3500)(mV)$$

The amplitude of output signal could be stable at 2V, when the amplitude of input signal is changed to 12 mV:

$$f(t) = 12 \times \sin(2 \times \pi \times 3500)(mV)$$



(a) A_i=100 μ V， f =3.5KHz



(b) A_i=12mV， f =3.5KHz

Figure10. The test result of AGC

After a period of AGC adjustment, the amplitude of output signal could still be stable at 2V. Test result is as shown in figure 10, the flatness of the output signal has been improved greatly. CH1 is the input signal, the output signal can be observed in the CH2.

Having been tested:

AGC compression ratio C =- 40dB.

The amplitude range of input signal ≥ 60dB.

The flatness of output signal $\leqslant$ 2dB.

E. Zero-crossing Detection Test

The paper gives a simulating result of zero-crossing detection to see the validity of algorithm. Sine signal $f(t)=\sin(400\pi t)+\sin(1000\pi t)$ is added into gauss white noise in 10 seconds, time-domain waveform is as shown in figure 11.

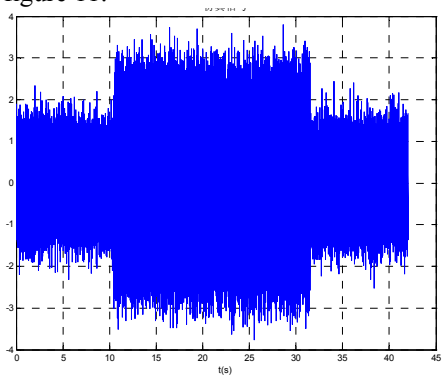


Figure11. Time-domain waveform in the zero-crossing detection

The curve of zero-crossing detection is as shown in figure12, the upper red curve is upper threshold for

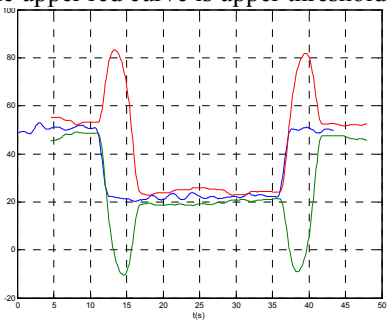


Figure12.The curve of zero-crossing detection

detection, the lower green curve is lower threshold for detection, and zero-crossing curve is the mid blue one. Because the frequency of sine signal is lower than gauss white noise, the zero-crossing times decrease in 10 seconds, we could see that early warning system give the alarm in 11.5 seconds, and withdraw the alarm in 36.5 seconds.

VI. Conclusion

The paper designed and implemented a digital signal preprocessor system. Compared with the conventional preprocessor system, the preprocessor system adopts digital design structure as much as possible and could be free from the shackles of hardware architecture, providing expandable hardware platform for signal processing software. The preprocessor system possesses a relatively flexible software packages to modify the hardware parameters which can only be adjusted by hardware changes in convention way. preprocessor system could meet the needs in the specific application condition by calling the appropriate function packages, avoiding the cumbersome caused by designing a new hardware of preprocessor system system, enhancing the versatility, flexibility and adaptability of preprocessor system. The preprocessor system has been applied in an underwater acoustic detection system successfully, its implementation lays a foundation for the realization of digital preprocessor system and has a good application prospect.

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