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High linear, High CMRR, Low Power OTA with Class AB Output Stage

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Abstract—This paper presents a linear Operational Transconductance Amplifier (OTA) that combines two linearization techniques, one with adaptive biasing of differential pairs and second with using of resistive source degeneration. OTA has ±0.9v power supply and consumes 250 µw. Improvement of adaptive bias circuit and using class AB output stage and CMFB circuit has enhanced the CMRR to 169dB in DC that reduces to 131dB at 1MHz. OTA has been simulated with TSMC 0.18µm CMOS technology in Hspice. The simulated third order harmonic distortion (HD3) with applying a 600mvP-P differential input is -65dB at 1MHz frequency.

***Index Terms*—Operational Transconductance Amplifier (OTA); linearity; adaptive bias circuit; source degeneration; CMRR**

I. Introduction

Operational Transconductance Amplifier (OTA) is a fundamental building block of analog circuits and systems. OTA has been used to implement many kinds of analog circuits such as; opamps, data converters, four-quadrant multipliers, mixers, modulators and continuous-time filters [1]-[16]. In such application as asymmetrical digital subscriber lines (ADSL) and cable-modem, the linearity has to be better than 60dB while for example, video applications require at least 60dB of linearity at 5MHz [2]. Gm-C topology that is a good choice for realizing continuous-time filter has better performance in frequency response and electronic tuning capability, but suffers from poor linearity [3], [4]. Thus designing an OTA with high linearity tends to be a constraint in circuits and systems design task.

In literatures several techniques have been presented to design linear transconductor blocks. In [5] utilizing a tail current that depends on the square of input differential signal, linearity in output current of strong inversion transconductor has been improved. This technique which is known as adaptive bias technique loses its performance due to second order effects in modern nano scale devices. Source/gate degeneration is another technique for linearity enhancement, specially in nano scale CMOS technology which the HD3 due to mobility reduction effect is considerable [2]-[4], [6]-[9]. However using high source degeneration factor (the product of the transconductance with the resistance) results in such drawbacks as; significant transconductance loss, excessive power consumption and enormous area usage [2].

Some other techniques use two or multiple Gm cell to cancel third order harmonic distortion [10], [11]. Double Differentia Pair (DDP) is one of these techniques that uses two cross coupled differential pairs. Then choosing proper sizing and tail current biases can cancel the third order harmonic. The main drawbacks of these techniques are higher power consumption and transconductance loss [2], [7], [13].

In this paper we combine both adaptive bias [5] and source degeneration techniques to improve the linearity of a transconductor. A well accurate-precise analog processing requires a pure wanted signal. This means that the wanted signal is best to be not only as distortion free as possible but also has to be as free as possible of any interference (common mode signal). Consequently to ensure the best processing condition besides providing a high linearity we have to provide a high CMRR too, the point which seems to be less regarded in most works so far. Therefore in this work the adaptive bias circuitry is improved to provide a largely high CMRR too. In section II we propose the principles and theoretical relations of these linearization techniques. In section III complete linear OTA and theoretical relations which approve CMRR improvement, is shown. In section IV simulation results are given and in section V we conclude the paper.

II. Principle of Linear Transconductor

Fig. 1 shows a source-coupled n-channel differential pair that is biased by current tail I_{SS}. In this figure *vin1* and *vin2* are input signals including both common and differential modes. The large-signal i-v transfer characteristic will be given by:

$$i_{out} = I_{D1} - I_{D2} = \frac{1}{2}\beta v_{in}\sqrt{\frac{4I_{SS}}{\beta} - v_{in}^{\ 2}} \quad |v_{in}| \le \sqrt{\frac{2I_{SS}}{\beta}} \quad (1-a)$$

$$I_{D1} - I_{D2} = I_{SS}\,\mathrm{sgn}(v_{in}) \quad |v_{in}| > \sqrt{\frac{2I_{SS}}{\beta}} \quad (1-b)$$

$$\beta = \mu_n C_{ox}\frac{W}{L} \quad , \quad v_{in} = v_{in1} - v_{in2}$$

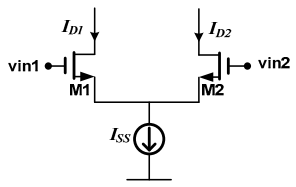

Figure 1. Simple differential pair.

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In (1) v_{in} is differential input (*vin1-vin2*) and "sgn" is sign function. Other parameters in (1) have their usual meanings. For realizing a linear relation between differential output current and differential input voltage, the result of radical in (1-a) should be a constant. This will be realized using a tail current containing a component dependent on the quadratic input v_{in}^2 to cancel the nonlinearity of the output current. So assuming $I_{SS} = I_{SS0} + k' v_{in}^2$ we get:

$$i_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\sqrt{\frac{4I_{SS0}}{\mu_n C_{ox} W/L} + \left(\frac{4k'}{\mu_n C_{ox} W/L} - 1\right) v_{in}^2} \quad (2)$$

In [5] biasing current, dependent to input signal has been implemented with cross coupled differential pair biased by constant separate current source. In this paper we use improved version of this adaptive bias circuit to achieve high CMRR too. Fig. 2 shows the improved adaptive biased transconductor. Adding M7 which is connected in series with diode connected transistor, (M8) for injecting signal-dependent current to common source node (B), results a higher CMRR as will be seen later.

In Fig. 2, the currents of M5, M6 transistors can be expressed as follows [5], [10]:

$$I_5 = I + I\left(-\gamma\left(v_{in}\sqrt{k/I}\right)^2 + \frac{\chi}{2}\left(v_{in}\sqrt{k/I}\right)\sqrt{1-\eta\left(v_{in}\sqrt{k/I}\right)^2}\right) \quad (3-a)$$

$$I_6 = I + I\left(-\gamma\left(v_{in}\sqrt{k/I}\right)^2 - \frac{\chi}{2}\left(v_{in}\sqrt{k/I}\right)\sqrt{1-\eta\left(v_{in}\sqrt{k/I}\right)^2}\right) \quad (3-b)$$

Where,

$$\chi = 4n/(n+1),\quad \eta = n/(n+1)^2,\quad \gamma = n(n-1)/(n+1)^2$$
$$k = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} \quad (4)$$

Sum of these currents depends on the quadratic input v_{in}^2as:

$$I_5 + I_6 = 2I + 2I\left(-\gamma\left(v_{in}\sqrt{k/I}\right)^2\right) = 2I + \left[2n(n-1)/(n+1)^2\right] k v_{in}^2 \quad (5)$$

Which is the same as $I_{SS} = I_{SS0} + k' v_{in}^2$ if $k' = \left[2n(n-1)/(n+1)^2\right]k$. To remove the nonlinearity in (2) we should have [5]:

$$\frac{4k'}{\mu_n C_{ox} W/L} - 1 = 0 \Rightarrow \frac{2k'}{k} - 1 = 0 \Rightarrow k' = \frac{k}{2}, n = 2.155 \quad (6)$$

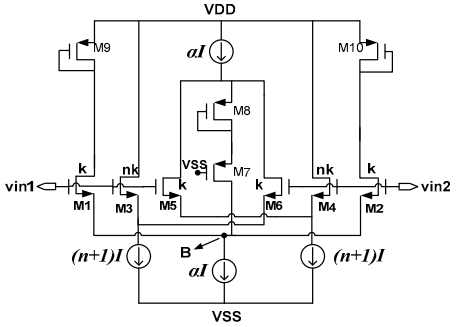

Figure 2. Improved version of adaptive biased transconductor.

For short channel devices the effective carrier mobility is a function of both the longitudinal and transversal electric fields. Considering the degradation of mobility due to these effects the drain current of a transistor in saturation region can be approximated as [14]:

$$I = \frac{k(v_{GS} - v_{th})^2}{1 + \theta(v_{GS} - v_{th})}(1 + \lambda v_{DS}) \quad (7)$$

Where, θ is the mobility reduction factor. From (7) The effect of θ can be interpreted as the use of a degeneration resistance of value $R_\theta = \theta/2k$ connected to source terminal. In Fig. 2, mobility reduction effect results in a tail current which depends also on forth power of input signal as equation (8)[1].

$$I_{SS} = I_{SS0} + k' v_{in}^2 + k'^3 R_{eq}^2 v_{in}^4$$
$$R_{eq} = \frac{\theta_n}{2k_n} + \frac{\theta_p}{2k_p} \quad (8)$$

Equation (8) shows that mobility reduction effect degrades the capability of adaptive bias technique in linearity improvement. Thus, for linearity improvement in this work, we use both adaptive bias and source degeneration techniques.

For simplicity we investigate the effect of source degeneration technique for decreasing HD3 in a simple differential pair. Ignoring second order effect, the output current of Fig. 1 can be described by a Taylor series expansion as follows:

$$i_{out} = I_{D1} - I_{D2} = \sum_{n=0}^{\infty} G_{M,(2n+1)} v_{in}^{2n+1} \quad (9)$$

Where, G_Ms are the coefficients of odd powers of the differential input voltage. Considering mobility degradation effect we will have:

$$G_{M,1} = \frac{1}{2}\frac{\sqrt{K_p (W/L) I_{SS}}}{1 + \frac{2}{\varepsilon_{crit}}\sqrt{\frac{I_{SS}}{W\,L\,K_p}}} \quad (10-a)$$

$$G_{M,3} = -\frac{G_{M,1}}{8\left(\frac{I_{SS} L}{K_p W}\right)\left(1 + \frac{2}{\varepsilon_{crit}}\sqrt{\frac{I_{SS}}{W\,L\,K_p}}\right)^3} \quad (10-b)$$

Where K_p is a technological parameter, ε_{crit} is the critical electric field, W is the width and L is the length of the transistors [9]. If two source degeneration resistors be added as shown in Fig. 3, the ac components of the output current approximately becomes:

$$i_{out} = \frac{G_{M,1}}{(1 + G_{M,1} R)} v_{in} + \frac{G_{M,3}}{(1 + G_{M,1} R)^4} v_{in}^3 \quad (11)$$

Relation (11) shows that HD3 is decreased by $1/(1+N_r)^3$, where $N_r = G_{M,1} R$.

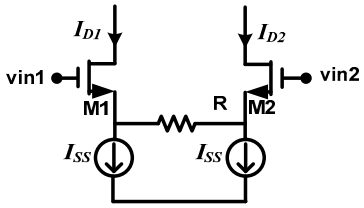

Figure 3. Source degeneration for linearity enhancement.

III. Proposed OTA

With reference to principles explained in section II the complete fully differential OTA which benefits from the source degeneration and adaptive bias techniques as well as a CMFB circuit is shown in Fig. 5. In this circuit α=4, n=2.16, I=10μA and I_{CSS}=10μA.

Output stage has class AB structure which results in low quiescent current for output stage and larger current transferred to loads. This class AB scheme enhances the gain of the OTA, 2 times and reduces the common mode gain, so results in higher CMRR. Using fully differential structure to achieve higher dynamic range, CMRR and PSRR, we need a CMFB circuit. CMFB circuit consists of two parts; common mode signal detector including M23-M30 as is shown in Fig. 4. It connects to main body of OTA at nodes "CMFB" (see Fig. 4 and Fig. 5). The second part of CMFB block includes M19-M22 (in Fig. 5) which are responsible for regulating the common mode voltage of OTA outputs.

A. Frequency Response

Dominant pole of the OTA at output nodes along with the much higher pole of the first stage at nodes "1","2" result in good stability. Class AB output stage also imposes a high frequency pole in node "X" and "Y" (see Fig. 5) which has negligible effect on frequency response of the OTA. Hence the poles of the OTA are as:

$$P_{d,(out)} = \frac{1}{(r_{O11} \| r_{O13} \| r_{O19} \| r_{O21}) \times (C_{P,out} + C_L)}$$

$$P_{nd(1,2)} = \frac{g_{m9}}{C_{p1,2}}$$

$$P_{nd(X,Y)} = \frac{g_{m15,16}}{C_{pX,Y}} \quad (12)$$

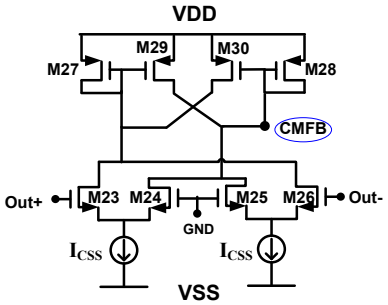

Figure 4. Common mode detector circuit

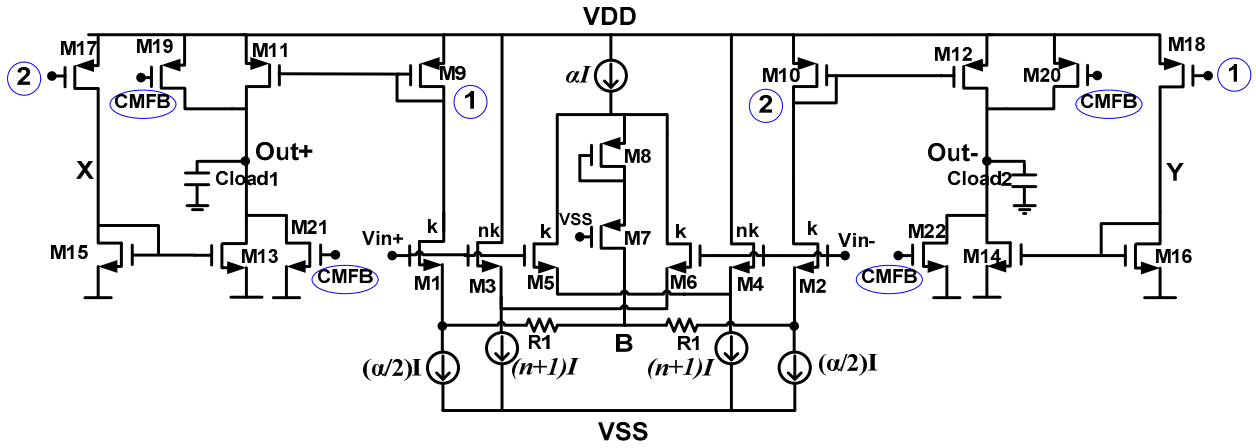

Figure 5. Proposed linear OTA

B. CMRR Improvement

Proposed OTA has high CMRR due to adding M7 and using class AB output stage and the CMFB circuit. To investigate the effect of M7 in CMRR improvement we consider common mode small-signal equivalent circuit for two states, without M7 and with it as is shown in Fig. 6. Writing KCL equations in A, X and Y nodes in Fig. 6-a, and in A, B, X and Y nodes in Fig. 6-b and assuming infinite value for current sources resistance (r_{OS1}=r_{OS2}=∞), the common mode small-signal current of M1 and M2 (I_{cm}) can be obtained for two states (without M7 and with it) as (13) and (14) respectively.

$$I_{cm} = g_{m1} \times \frac{\frac{2}{r_{O5}}\left(\frac{n}{n+1}\right)}{2g_{m1} + \frac{2}{r_{O5}}\left(\frac{n}{n+1}\right) + \frac{4g_{m1}}{r_{O5}g_{m8}}\left(\frac{n}{n+1}\right)} \times v_{cm} \quad (13)$$

$$I_{cm} = g_{m1} \times \frac{\frac{1}{r_{O7}} + \frac{2}{g_{m8}r_{O5}r_{O7}} - \frac{2}{r_{O5}}}{\left(g_{m8} + \frac{2}{r_{O5}}\right)\left(T + \frac{1}{g_{m8}r_{O7}}\right) + \frac{2g_{m1}g_{m8}}{g_{m7}} - \frac{T}{r_{O5}}\frac{2g_{m5} + \frac{2}{r_{O5}}}{g_{m3} + g_{m5}}} \times v_{cm} \quad (14)$$

Where,

$$T = -2g_{m1}\left(\frac{1}{g_{m7}} + \frac{1}{g_{m8}g_{m7}r_{O7}} + \frac{1}{g_{m8}}\right) \quad (15)$$

In (13) and (14) v_{cm} is common mode input voltage, r_O is small-signal drain-source resistance ($\partial v_{DS}/\partial i_D$) of transistors. CMRR can be obtained as:

$$CMRR = \frac{A_d}{A_c} = \frac{\frac{g_{m1}}{(1+g_{m1}R_1)g_{m9}} \times \left(g_{m11} + \frac{g_{m12}}{g_{m14}}g_{m13}\right) R_{out}}{\frac{I_{cm}}{v_{cm}g_{m9}} \times \left(g_{m11} - \frac{g_{m12}}{g_{m14}}g_{m13}\right) R_{out}} \times A_{V,CMFB} \quad (16)$$

Relation (16) shows the great achievement of the possibility to drastically reduce A_C by properly adjustment of g_{m11}-g_{m14}. Ideally if the related term in the parenthesis of the denominator become zero, make the CMRR to become infinite.

In (16) $A_{V,CMFB}$ is the gain of CMFB circuit which is given in (17) and I_{cm}/v_{cm} can be obtained from (13) and (14) for two states; without M7 and with it, respectively.

Equation (17) shows that using positive feedback in the load of the common mode detector circuit, results in high gain for this circuit. The closer be the conductance of M29 to M27 the higher would be the $A_{V,CMFB}$ and consequently the higher would be the CMRR. But, however an appropriate difference between g_{m27} and g_{m29} should be regarded to avoid instability in common mode feedback loop.

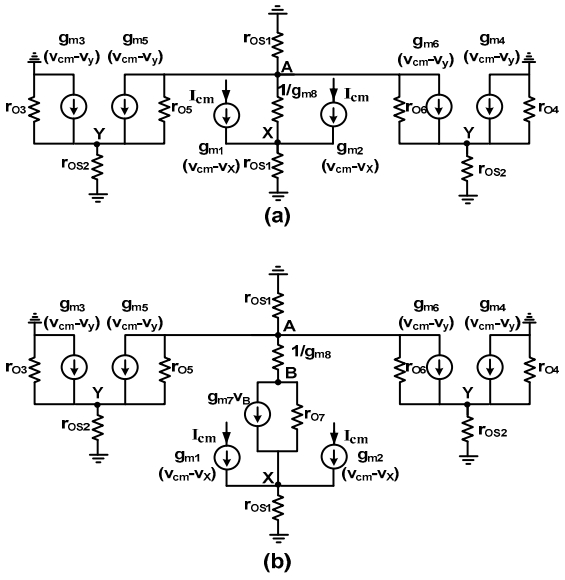

Figure 6. Common mode small-signal equivalent circuit for: (a) without M7. (b) with M7.

$$A_{V,CMFB} = \frac{-2g_{m23}}{g_{m27} - g_{m29}} \times (g_{m19} + g_{m21}) R_{out} \quad (17)$$

In (13), sizing M7 such that $1/r_{O7}+2/(g_{m8}r_{O5}r_{O7})=2/r_{O5}$ causes I_{cm} to become zero, giving high value for CMRR. This condition can be simplified as $r_{O5}/r_{O7}=2$ and assuming level 1 model, can be written as $I_7L_5/I_5L_7=2$ where I is bias current and L is the length of transistors. Simulation results show that improved version of adaptive bias circuit increases CMRR more than 60dB.

IV. Simulation Results

The proposed OTA (Fig. 5) have been simulated using the standard 0.18µm TSMC CMOS technology in Hspice simulator. Power supply of the circuit is ±0.9v and OTA consumes 250µw. Open loop DC gain of the OTA is 42dB and with 10pf load capacitances connected between outputs and ground, GBW becomes 3.2MHz with 90º phase margin. Fig. 7 shows the magnitude of the frequency response. Applying an input signal with 1MHz frequency, HD3 of output voltage versus magnitude of input signal is shown in Fig 8-a. Fig 8-b shows the value of peak-to-peak differential output voltage.

Fig. 9 shows CMRR versus frequency. As this figure shows CMRR in DC is 169dB and reaches to 131dB at 1MHz. Table I shows the main specifications of proposed OTA compared with some similar works.

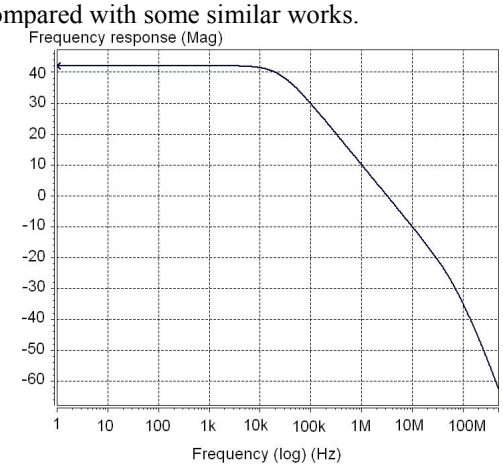

Figure 7. Frequency response of OTA

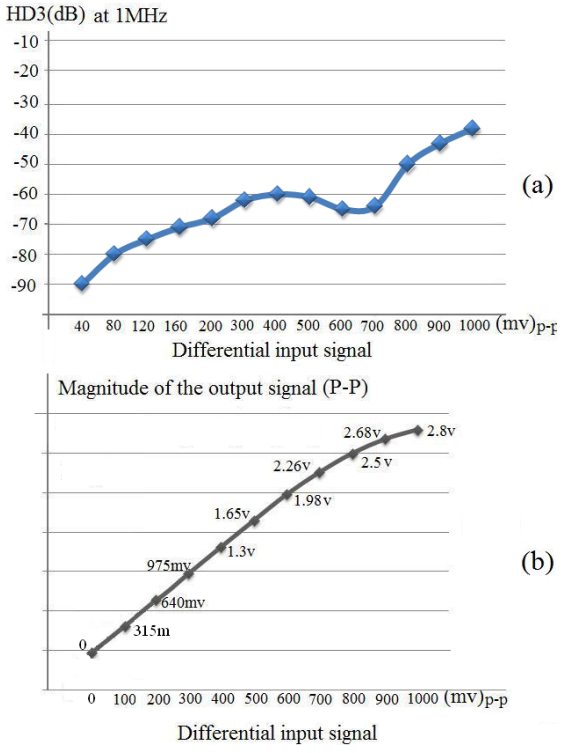

Figure 8. (a) HD3 of output voltage. (b) Amplitude of peak-to-peak differential output voltage.

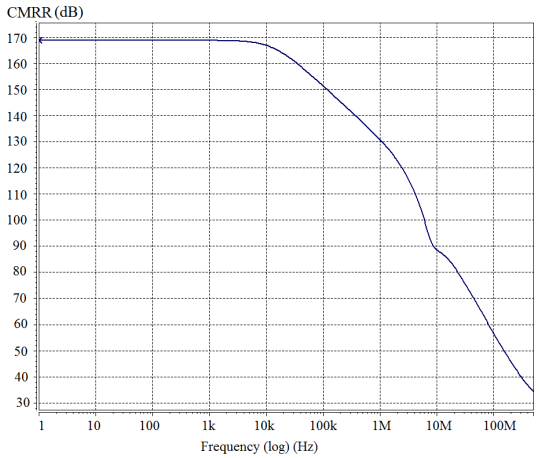

Figure 9. CMRR versus frequency of input signal.

TABLE I. SPECIFICATIONS OF PROPOSED OTA COMPARED WITH SIMILAR WORKS.

Specification	**This work 0.18µm**	**[9] 0.35µm**	**[11] 0.18µm**	**[15] 0.18µm**	**[16] 0.5µm**
Supply voltage	±0.9v	3.3v	1v	1.8v	±1.1v
Power dissipation	250µw	10.3mw	2.5mw	145µw	410µw
DC gain	42dB	31.5dB	NA	NA	63dB
CMRR(DC)	169dB	56.5dB	NA	NA	108dB
Transconductance	76µS	1.05mS	1000µS	20 µS	NA
Linearity	HD3= -65dB 0.6vp-p at 1MHz	IM3= -80dB 0.7vp-p at 30 MHz	HD3= -55dB 0.4vp-p at 50MHz	HD3= -65dB 0.6vp-p at 1MHz	THD= -62dB 1vp-p at 100KHz

NA. Not Available

V. CONCLUSION

In this paper we proposed a highly linear OTA which combines two linearization techniques. An improved Adaptive bias circuitry is used to achieve high CMRR and source degeneration is utilized to improve the linearity in nano scale CMOS technology. Due to using class AB output stage, the quiescent current of this stage is low which results in low power consumption. OTA has been simulated with TSMC 0.18µm CMOS technology in Hspice. The simulated third order harmonic distortion (HD3) with a $600mv_{P-P}$ differential input is -65dB at 1MHz. CMRR of the OTA is 169dB in DC up to 10KHz which then rolls off down to 131dB at 1MHz.

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